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USSR Report

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

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23 February 1984

USSR REPORT

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

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GENERAL

UDC 681.3

STATUS OF SCIENTIFIC RESEARCH IN FIELD OF COMPUTER TECHNOLOGY IN COUNTRY'S VUZES

Leningrad IZVESTIYA VYSSHIKH UCHEBNYKH ZAVEDENIY: PRIBOROSTROYENIYE in Russian No 9, Sep 83 pp 5-9

[Article by Doctor of Technical Sciences, Professor Yu. M. Smirnov, chairman of section "Computer Technology," Scientific and Technical Council, USSR Ministry of Higher and Secondary Specialized Education, Moscow Higher Technical School imeni M. E. Bauman]

[Text] The basic directions of scientific research in the field of computer technology are considered and their status is evaluated. Examples of practical realization of vuz research in the academic process and in industry are given.

Computer technology now largely determines the rates of scientific and technical progress. Scientists of higher schools make an important contribution to scientific research in the field of computer technology. The higher school considerably expanded research on the most important problems of computer development and computer use in the national economy during the 11th Five-Year Plan, along with training of scientific and engineering personnel. Completion of the tasks posed by the party at the 26th Congress in computer technology requires that scientific research be concentrated in the basic directions of its development, an increase in the effectiveness of developments and the most rapid introduction of the results of investigations into the national economy. The basic directions in computer development have been reflected in the Coordination Plan of the Scientific Research of Vuzes in the Field of Computer Technology for 1981-1985, confirmed by order of the USSR Minister of Higher and Secondary Specialized Education.

The coordination plan contains the following sections: design of highly efficient computers and systems, improvement of the software and programs for computers and systems, design and production of computers and systems and organization of computing processes.

The main problems of the first section are: development of the structures and operating principles of promising computers, development of the theory and design principles of high-performance specialized computer systems, investigation and development of promising input-output data systems, investigation of

the design principles of highly reliable computers and systems and so on. Investigations in this direction, of important significance, are being conducted by many vuzes, among which is the Kiev Polytechnical Institute, where the design principles of ultrahigh-performance recursive conveyor computer systems of broad designation are being developed. The significance of this research includes the capability of working with a variable set of machine operations of arbitrary complexity, which contributes to simplification of user programs and determines high efficiency for applications of computers in different areas of the national economy.

The party and government have recently been devoting a great deal of attention to development of investigations in machine automation, equipping devices that use microprocessors and development on this basis of automated enterprises and production complexes. The development of production and support of wide applications of built-in automatic control systems using microprocessors and minicomputers that permit large-scale use of high-performance energy- and materials-conserving techniques in the national economy and that considerably increases the reliability of the produced equipment and the quality of the produced products occupy a special position in this regard.

Scientific research at vuzes in the field of microprocessor technology is being conducted in the following directions:

development of the component base of microprocessors (Moscow Engineering Physics Institute and Moscow Institute of Electronic Equipment, Leningrad Institute of Precision Mechanics and Optics, Yerevan Polytechnical Institute and so on);

development of new classes of highly efficient microcomputers and microprocessors (Leningrad Electrotechnical Institute imeni V. I. Ul'yanov (Lenin), Moscow Aviation Institute, Belorussian State University, Kaunas and Donskoy Polytechnical Institutes and so on);

development of methods and devices for design of microcomputers (Moscow Institute of Transport Engineers, Kharkov Polytechnical Institute, MIFI [Moscow Engineering Physics Institute], MAI [Moscow Aviation Institute], LETI [Leningrad Electrotechnical Institute imeni V. I. Ul'yanov (Lenin)] and so on);

development of high-performance multiprocessor systems (Moscow Institute of Electronic Machine Building, Novosibirsk Electrotechnical Institute, Taganrog Radio Engineering Institute and so on).

The coordination plan includes tasks of improving the software and programs for computers and systems. They include: development of systems programming theory, development of methods of organizing computing processes that provide efficient use of computer resources, development of a multilanguage programming system, development of applied program packages for simulation of dynamic processes, development of programs for design automation, developpent of general and special software for computers and complexes based on YeS computers, development of computer software for process control, development of autonomous and collective-use operating systems for microcomputers, development of applied program packages for training purposes and so on.

According to the coordination plan, a two-machine complex based on the YeS-1033 with common disk memory was developed and the OS 6.1 operating system was expanded at Leningrad State University, which provided input of a package of tasks for two computers through a single input console, which permits an increase in the labor productivity of programmers. The programs for the TS-7971 group control device, which is included in the YeS-7970 display complex, was developed within the framework of this research, conducted by decision of the GKNT [State Committee for Science and Technology]. The developed software passed state trials and the developers were awarded with medals of VDNKh SSSR [Exhibition of achievements of the national economy of the USSR].

An important task of the 11th Five-Year Plan is solution of processes of "automation of design and scientific research work using computers." To solve this problem, many vuzes are concentrating their attention on development of applied program packages to automate simulation of complex systems (the Moscow Engineering Physics Institute and so on) and for computer design automation (the Penza Polytechnical Institute, Moscow Power Engineering Institute, Perm State University and so on). Investigations are being conducted in development of software for design automation of probabilistic converters and a programmable processor with interactive capabilities (Kazan State University and so on) and software programs of interactive systems are being developed for automation of scientific research (Kuybyshev State University, Moscow Higher Technical School imeni N. E. Bauman and so on). A great deal of attention is being devoted to the problems of software development for mini- and microcomputers.

The scientific research conducted at vuzes is inseparably linked to the training process, the current status of which is determined by widespread use of the methods and devices of computer technology. Development and use of diverse applied program packages for improvement of specialist training have been suggested as a result of investigations in this direction (Perm Polytechnical Institute, Tomsk State University, Leningrad Shipbuilding Institute, Moscow Institute of Steel and Alloys and so on). Automated teaching systems based on YeS computers are being developed (Kazakh Polytechnical Institute, Kazan State University, Riga Polytechnical Institute and so on).

The display input-output hardware and software developed at the Leningrad Electrotechnical Institute imeni V. I. Ul'yanov (Lenin) is used in course design and in practical studies of students in specialty 0647--"Applied mathematics," in outline of the courses "Methods and algorithms for computer processing of signals," "Machine graphics and interactive systems," "Methods and algorithms for processing measuring data" and so on. Investigations in development of design and production of computers, which comprise the third section of the coordination plan, are of important significance for development of computer technology. Scientific research in this direction is combined into two main problems: "Investigation in the field of creating computer components and assemblies that operate on new principles" and "Applications of computers for automated design of computer equipment and development of its manufacturing technology."

Among the interesting problems should be included the work of the Irkutsk Polytechnical Institute on investigation of the mechanism of charge transfer

in amorphous polymer organic semiconductors and the investigations conducted at the Moscow Engineering Physics Institute on development of functional microelectronic assemblies based on charge-capacitance devices. Investigations of the Kishinev Polytechnical Institute in development and introduction of an automated design system for alloys and resistive microassemblies based on them are of specific significance in development of computer production technology. The prospects for development of science and acceleration of technical progress require extensive scientific research in the direction of organization of computing processes. Problems of development of collective-use networks and computer centers, which comprise the fourth section of the coordination plan, are significant in this case. The essence of the direction is revealed in the following basic problems: "Investigation and development of the architecture of computer networks" and "Development of methods of operation and control of computer networks." Moscow State University, the Moscow Higher Technical School imeni M. E. Bauman, the Moscow Aviation Institute, the Moscow Engineering Physics Institute, the Moscow Power Engineering Institute, Gorky State University, Belorussian State University and so on are participating in the scientific research. The investigations of the Leningrad Forest Engineering Academy are directed toward development of the scientific bases of operation of computers and systems. The investigations of the Moscow Institute of Electronic Machine Building are oriented toward development and creation of computer networks.

Terminal classrooms based on the Elektronika-60 have been created to work out operator-computer interactive devices and also methods of teaching the fundamentals of automation of scientific research (Novosibirsk University and the Novosibirsk Electrotechnical Institute). Measuring computer complexes based on the SM-3 and SM-4 computer, CAMAC devices and systems software designed to teach the fundamentals of automated systems design for scientific research, have been put into operation (LETI and Kuybyshev Aviation Institute). Moreover, systems for teaching the fundamentals of experimental data processing based on the DZ-28 microcomputer were developed within the framework of the integrated program of the USSR Academy of Sciences and the RSFSR Minvuz "Automation of scientific research" (Moscow Physicotechnical Institute and Petrozavodsk State University).

The problem of increasing efficiency in use of computer equipment has always been timely. However, whereas main attention was devoted several years ago to increasing the quantitative indices of computer operation, problems of qualitative use of computer equipment are now timely. The essence of the problem includes the question of whether to solve problems on a computer that correspond to the capabilities of the machines. The problem of improving the qualitative indices of computer operation is related mainly to development and improvement of modern systems and to provision of extensive practice in the use of computers by all instructors, students and scientific colleagues of vuzes. An example of computer use is Moscow State University, where a collective-use computer center has been created, which considerably expanded the capabilities of computer use in the training process and in scientific research. Applied program packages and interactive interpreters from high-level languages have been developed. The ShAR-BESM6 program complex, which permits study of the parameters of flow around bodies without the use of a

wind tunnel and so on, has been developed. Software for the DUVZ system (interactive remote task input system) was developed at MVTU imeni M. E. Bauman, which considerably expanded the capabilities of computer use in the training process and found application at a number of enterprises. A number of vuzes of the Scientific Association of the RSFSR Minvuz, jointly with the USSR Academy of Sciences, are conducting investigations on automation of scientific research and in development of systems and software for automation of monitoring the processes of testing objects of new equipment. The Riga Polytechnical Institute has turned over for experimental operation the first unit of the Kontakt teaching system for study of general engineering disciplines: physics, chemistry, algorithmic languages and so on. However, some vuzes (for example, the Tbilisi and Kiev State Universities, Lvov Polytechnical Institute and so on) are still incapable of efficient use of computers. This is explained by a number of factors:

the experience of the best vuzes is inadequately transferred to the remaining vuzes, which requires improvement of methodical support, especially for the vuzes of outlying regions;

the sector fund of algorithms and programs is functioning poorly;

the technical base at a number of vuzes is clearly inadequate.

The competition for better use of computer equipment at the vuz should be of important significance in increasing the efficiency of utilization of computer equipment. The status of the competition, which is now in the confirmation stage, provides for an estimate of the accrued machine time, selection of the most efficient organization of the computing process on a specific technical base, the quality of scientific problems to be solved, the level of computer use in the training process and so on. An important problem for increasing the efficiency of scientific research and improvement of its use at vuzes is coordination of scientific research work of vuzes in the field of computer technology. The coordination plan was compiled for this and a coordination council has been confirmed, the functions of which include the development of methodical problems in coordination of scientific research work in the field of computer technology, preparation of proposals on basic scientific directions, integrated programs and plans of scientific research of vuzes in the field of computer technology, preparation of proposals for accelerated introduction of the results of research according to the coordination plan into the national economy and the training process. The scientific research of the higher schools in the field of computer technology, directed toward solution of timely scientific problems, is being conducted at more than 100 of the country's vuzes in all the union republics. They have a rather high scientific level and the results are finding wide practical application, which determines their worthy contribution to fulfillment of the national economic tasks of the 11th Five-Year Plan.

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PROBLEMS OF IMPROVING MANAGEMENT OF USE OF COMPUTER TECHNOLOGY IN HIGHER SCHOOLS

Leningrad IZVESTIYA VYSSHIKH UCHEBNYKH ZAVEDENIY: PRIBOROSTROYENIYE in Russian No 9, Sep 83 pp 10-14

[Article by A. Ya. Savel'yev, N. M. Kogdov, B. A. Sazonov and S. E. Luk'yanov, Moscow]

[Text] The need to account for, monitor and analyze the efficiency of computer use in the higher schools is substantiated and the software of the subsystem "Computer technology," used in the OASU [automated sector management system] of the Minvuzes of the union republics and of the USSR Minvuz, are described.

A knowledge of computer technology and skills in use of it in practical activity are some of the important indices of the skill level of the modern specialist. Therefore, the presence of computers at vuzes and their use in training work have become an inseparable part of the teaching techniques in the higher schools.

Analysis of the status of the use of computer technology at vuzes from the results of the 10th Five-Year Plan indicates an increase in the indices of outfitting vuzes with computer equipment and an increase of the efficiency of computer use. Many vuzes are working fruitfully on development of new promising forms of computer use in the training process, the main ones of which are:

checking, automated teaching, computer practical courses, modelling, course and thesis design work and so on. The nature of the problems solved by students on computers is becoming more and more research and creative that requires non-traditional approaches to planning and design, research and calculating work. The number of academic disciplines taught at the vuzes and completion of course and thesis projects, which are unthinkable without the use of computers, is growing. Problems of this class include those of finding optimum solutions, selection of versions for determination of local extreme values, solution of planning and design problems by mathematical and simulation modelling methods and so on. At the same time, there are serious deficiencies in equipping the vuzes with computer equipment and use of it. Standards of the average daily operating time of computers are still not being met at some vuzes and the coefficient of utilization of some peripheral devices and data preparation devices is low.

The existing distribution in the use of machine time can also not be recognized as satisfactory when only an average of 30 percent of the annual fund of computer machine time is being expended on the training process in the higher schools, whereas 60 percent or more of machine time is being expended on scientific work. The load of computers with tasks of an academic nature is still low. The absence of an efficient centralized accounting and distribution system of computer technology makes it difficult to manage its use at vuzes on the part of USSR Minvuz.

It has been proposed that the stock of computers of vuzes be considerably renovated and expanded during the 11th Five-Year Plan, mainly by modern high-performance models of YeS and SM computers. The number of mini- and microcomputers, microprocessor equipment and peripheral devices, including display stations and data teleprocessing devices, delivered to vuzes is increasing significantly, which permits an expansion in work to create collective-use computer systems at vuzes. Creation of collective-use systems provides further development of traditional forms and the appearance of new forms of computer use at vuzes, such as automated control, teaching and monitoring systems, experiment automation systems, information and reference systems and so on. A specific program, directed toward expansion and increasing the efficiency of computer use in the training process and in scientific research, was adopted in July 1981 by the board of the USSR Minvuz. The program provides a wide range of measures to correct deficiencies in the use of computer technology in the country's vuzes, including a complex of measures to improve the control system for use of computer technology in the higher schools. The main ones are improvement of the accounting and analysis system for efficiency of computer use in vuzes, development of means to determine and forecast the needs of vuzes for computer technology and improvement of the computer technology distribution system in the higher schools.

Solution of these problems leads to freeing of workers of the USSR Minvuz and the minvuzes of the union republics from routine labor in processing the accounting data of vuzes, improvement in monitoring the activity of vuzes and of subordinate organizations and an increase in the quality of analysis and planning of the activity of vuzes. Organizationally, an automated control system for the use of computer technology in the sector should have the traditional three- and four-level structure: the USSR Minvuz, the minvuzes of the union republics and the main administration of vuzes of the USSR Minvuz, regional computer centers and vuzes. The system should provide solution of the following functional subproblems: creation and management of an accounting and statistical data file on the presence and use of computer technology in the sector, issue of output periodic accounting forms, analysis of the efficiency of use of computer equipment (SVT), determination of the need for computer equipment and of material and technical resources, distribution of computer equipment, prediction of the development and use of computer equipment in the sector and data transmission to OGAS [Statewide automated system for collection and processing of information for accounting, planning and control in the national economy].

The automated control system for use of computer technology in the higher schools is technically being realized on the basis of the OASU subsystem of the USSR Minvuz "Computer technology," development of the first stage of which was completed in 1981 by the Scientific Research Institute of Problems of Higher Schools (NIIVSh). The subsystem "Computer technology" is a functional subsystem of the first stage of the OASU of the USSR Minvuz and is intended for solution of problems of gathering, classification and processing of information about the presence and use of computer technology at vuzes and also about the efficiency of operating it. Introduction of this subsystem will make it possible to estimate with sufficient accuracy the status of equipping the vuzes with computer technology and to determine the need for it during the planning period. The first stage of the subsystem "Computer technology" solves problems of creation of an information database about the presence and use of computer equipment in the sector, publishing of a set of periodic accounting forms and analysis of the efficiency of computer use in the sector. Moreover, the subsystem is capable of performing information reference functions in solution of problems of determining the need of vuzes for computer equipment and of the distribution of computer equipment among vuzes. The software of the subsystem "Computer technology" is being realized by the programs complex of the automated data processing system (ASOD) Mars, developed at NIIVSh, which is the basis system used for design of functional ASU subsystems of the higher schools (VSh). The subsystem "Computer technology" is informationally compatible with other functional subsystems of the ASU of higher schools and can be introduced and used together with them. The information file of the subsystem "Computer technology" is filled with data coming from the vuzes. The information card of the subsystem, filled out annually by the vuzes, contains address data, identification codes of the vuz, summary data about the presence, receipt and write-off of computer equipment and developed data about digital computers. Moreover, the information card contains data about leased computers and about those planned for delivery.

The presence of such detailed, annually updated data in the subsystem "Computer technology" makes it possible to provide interested management personnel of USSR Minvuz and the minvuzes of the union republics with diverse information of the required degree of detail, needed for effective management of the use of computer technology at vuzes. The information cards of the subsystem "Computer technology," filled out at the vuzes, are sent to the GIVTs [Statewide Information Computer Center] of the corresponding minvuzes of the union republics, where they are punched, checked and entered in the information array. An album, consisting of 14 periodic output accounting forms, is published on the basis of the created file. This album is used by the workers of the corresponding services of the minvuz of the union republic. A copy of the album of output forms and a copy of the information file are transmitted on magnetic tape by all the GIVTs of the minvuzes of the union republics to the IVTs [information computer center], NIIVSh, USSR Minvuz. All the received information files are combined at the IVTs, NIIVSh and an accounting statistical data file about the presence and use of computer technology in the sector is created. An album, consisting of 10 periodic output accounting forms, which is used by the workers of the corresponding services of USSR Minvuz, is published on the basis of this file.

Besides albums of the periodic accounting forms, the ASOD Mars makes it possible to obtain other non-standard output forms from requests of the corresponding services of USSR Minvuz and of the minvuzes of the union republics. In 1981 the first unit of the subsystem "Computer technology" underwent experimental operation at NIIVSh. The information card of the subsystem was sent to all subordinate vuzes. The results of processing these data, generalized for the republics and vuzes of the Main Administration of Vuzes, USSR Minvuz, were presented to the USSR Minvuz. The question "On improvement of the system for accounting and analysis of efficiency in use of computer technology at the country's vuzes" was considered at a meeting of the board of the USSR Minvuz in January 1982, at which the decision was made to create an automated system for accounting and analysis of efficiency in use of computer technology in the sector and of introduction of it into industrial operation in 1983. The output forms of the subsystem "Computer technology" offer integrated information to the user about the number and types of computer devices of vuzes, support of them with material and technical and human resources, production areas and about the conformity of the operating indices to norms confirmed by the USSR Minvuz and the USSR TsSU [central statistical administration]. Moreover, the output forms contain data that characterize the composition of computer users, the distribution of machine time among academic work, NIR [scientific research work] and ASU, data about the number and composition of the computer equipment written off and acquired annually by vuzes. The presence of the enumerated information permits rather complete analysis of the total state of affairs in the use of computer equipment at vuzes and determination of the best and worst vuzes and republic ministries. It becomes possible to solve on a reasoned basis the problems of determining the need of vuzes for computer equipment, the priority of outfitting vuzes with computer equipment and determination of the specific structure and composition of vuz collective-use computer centers.

Development of the software and programs for automated solution of such planning and management problems as determination of the need of vuzes, regions and republics for computer equipment, the distribution of acquired computer equipment among vuzes, forecasting the development and use of computer equipment in the sector and so on, was begun at NIIVSh in 1981 within the framework of investigation on the second unit of the subsystem "Computer technology."

The analysis showed that the information base of the subsystem "Computer technology" is insufficient to solve these problems. There is a need to use the information bases of other functional subsystems of OASU of USSR Minvuz such as "Vuz certificate," "Specialist training" and "Automated monitoring of developments of ASU VSh." Moreover, the problem of making decisions under conditions of the partial absence of information arises. Therefore, the second stage of the subsystem "Computer technology" uses the integrated information base of several subsystems. As is known, the ASOD Mars processes only a single information file; therefore, primary attention was devoted to development of means of access to any number of information files created by ASOD Mars devices. These universal devices were developed. The developed access devices can be used in programs written in high-level algorithmic languages (FORTRAN and PL/1). The use of these languages permits application of their powerful computing capabilities for solution of complex optimization problems of planning and management, solution of which is impossible by using the ASOD Mars.

It has been suggested from the results of industrial operation of the subsystem "Computer technology" that OASU of the USSR Minvuz annually summarize the results of the use of computer technology at vuzes at the meeting of representatives of the minvuzes of the union republics and that measures be planned to further increase the efficiency of its application.

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DISCARDED COMPUTER

Moscow SOTSIALISTICHESKAYA INDUSTRIYA in Russian 3 Sep 83 p 2

[Letter from A. Karnaukha, docent at the Dnepropetrovsk Metallurgical Institute imeni L. I. Brezhnev, and S. Gruzdyakov, laboratory chief, Dnepropetrovsk]

[Text] There are a number of orders and directive letters from the USSR and Ukrainian ministries of higher education aimed at improving students' preparation in mathematics and applying computer technology in the schooling process. They are in the spirit of the times: today's engineer must not merely know computers but also be able to use them. Furthermore, he must know how to present a problem to a programmer and be able to converse with computer scientists on more than a rudimentary level. All of this, of course, requires more than just lectures; there must also be practical work with computers.

Such work began about 20 years ago, when mini-computers of the "Promin'", "Mir", and "Nairi" types began to be used in the VUZes.

The friendliness of these computers was judged to be high by both teachers and their students. Their small size and simple programming language enabled this technology to be used in departments and laboratories and in work with theses and term papers. Of no small importance was the fact that there were no problems getting this equipment repaired. A maintenance organization was called, and in 1-3 days the computer would be up again.

Thus, this equipment was widely used at the VUZ level until 1980, when the republic organization in charge of repairs, "ZapadEVMkompleks," made the transition to servicing the new generation of computers; already by the end of 1982 the earlier mini-computers were no longer accepted for repair by any of the repair subdivisions in the Ukraine.

A question arose immediately: production of these mini-computers was ended in 1980, but their minimal operability was 10 years. What should be done? Should they be written off? They should not, from an economic standpoint: a computer costs 30,000 rubles, while repairs cost 150-200 rubles. It should continue to work a good deal longer!

But no, the comrades from "ZapadEVMkompleks" (Director M. Trofimchuk) advise that they be, in fact, written off. They even promise help in doing this. They say, get new computers to replace the old ones, and learn how to use them. To which we add that this takes up to two years.

But perhaps there are no spare parts for the mini-computers? There are. Industry is producing the same resistors, transistors, condensers as before. So what is the problem? Why move so precipitously to renew the stock of computers? The old ones might at least be used to justify the resources spent on them; then they could be written off.

One other snag. Previously, the "Nairi-K" computers were repaired for us by the Lvov Plant for Computer Maintenance (Director L. Gorbatovskiy). Now, having moved over to the "Ukrschettekhnika" association, the plant refuses to do this because the earlier price list for such work has been cancelled and a new one not issued.

What can be done? Have the department hire its "own" specialist for equipment repair and pay him 230 rubles a month (this is how they are paid in the centralized organizations) for occasional work? This does not make sense, and finding someone to do this work for less pay would be difficult.

But throwing out a good computer is simply a shame. Can't a guardian be found for a homeless computer?

12488
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COMPUTERS ON THE JOB

Moscow IZVESTIYA in Russian 17 Sep 83 p 2

[Article by B. Konovalov, special correspondent for IZVESTIYA, Novosibirsk, "A Computer at Every Work Station"]

[Text] Three years ago, an unusual building arose at Novosibirsk's Akademgorodok. Its metal luster contrasted sharply with the traditional stone structures on Lavrentev Prospect. At first, everything went as usual at this construction site: the bulldozers cleared the ground, and the foundation was laid. But then, the metal prefrabricated structure quickly went up.

The powerful "Sibakademstroy" was represented at this site by only the foreman and two engineers. The remaining workers were all from the laboratories of the Institute of Automation and Electrometry. The institute's work today is particularly important for the country, so the scientists did not want to wait any longer for "builders' favors".

"In all, we've built about 3,000 square meters of special purpose production space, practically with our own hands," I am told by the director of the academy's institute Yuriy Yefremovich Nesterikhin with obvious pride. "The basement is entirely devoted to optical and laser laboratories, technological installations and controlled computers. Above, in the center, are powerful machines of the "Ryad" system. And on the edges of this "computer center" are different laboratories. This design was chosen to bring specialists closer to the computers."

I take a look at how the developers of the electronic units are working. Automated work stations have been created for them.

First, the basic logic diagram is written by hand. Then, when it is chosen, the designer goes to an automated work station, to the "Plotting board" system, the so-called plotter-coder.

This basically is the Kuhlman drafting unit of the designer of the electronic age. The designer makes his sketch with a ball point pen set into the center of a plastic rectangle moving easily in any direction by means of wires.

The computer, meanwhile, codes his actions. When the work is finished, the designer easily switches the system to the opposite mode by the simple flick of a switch. Now, the computer itself draws the blueprint on a clean piece of paper. The designer must check whether the machine correctly "understood" him, after which the blueprint is stored in the computer memory.

At the automated work site of radio engineers, who must convert it into the technological language, the block's circuit is displayed on a screen resembling a color television. Under the screen is a keyboard, as on an ordinary typewriter. The engineer uses it to converse with the machine: not in a special mathematical language, but in a simple one understandable to any person. Pressing the keyboard to move a cursor over the circuit, the engineer gives the machine instructions: this wire end must be connected with that one. The machine itself chooses the minimum distance.

When the manufacturing stage arrives, some of the work, such as drilling holes for connecting wires, is done automatically by a machine with program numerical control. It is controlled by the commands of the computer, which is directed by the blueprint stored in its memory.

The finished electronic unit is returned to the designer for checking and adjustment. There are few who succeed in doing everything successfully the first time. Having detected the mistakes, the engineer returns to the display. Pressing the necessary key, he activates the "Edit" mode, and makes the corrections to the image.

Man and computer actively interact in the work process in this case. At any time, the engineer can order the machine to do what he needs. Not long ago, the opinion was that everyone would send their problems to powerful computer centers, where the mathematician specialists would solve them and return the answer. But the main road of automation has turned out otherwise. The focus now is on enabling any specialist--scientist, engineer, designer, technician--to use the computer's services at his own work site. Figuratively speaking, not to go to the computer center as to a well for water, but to have a pipeline. All one needs is to open the tap and use it.

The institute primarily uses automated technology to create systems for automating scientific research and industrial processes from modules of the international standard CAMAC. The people of Novosibirsk were among the pioneers in this efficient automation trend.

CAMAC's strength is that it enables the creation of automation systems to be switched to an industrial basis. Using designer terms, it's the block construction principle. A high-capacity integrated home-building factory is first built, which turns out standard functional blocks. Very different automation systems are built from them, depending on the need. For instance, for machines with numerical program control and for various tests: instruments, assemblies and machines; for directing industrial processes; and for processing data in any scientific experiments.

A unified bus transfer system developed at the institute enables the CAMAC to be linked with any computer, and its capabilities used for control or data processing. The electronics industry is currently expanding serial production of microprocessors. In particular, the small "Elektronika-60" is popular. The people of Novosibirsk are now extensively using it for their systems, by connection with the CAMAC. The "MIKRO-CAMAC.LAB" hybrid system has appeared, which serves as a personal laboratory computer.

The institute is readying production of a complex for automating vibration acoustic tests, which are very widely used. The compact system, called "Yenisey", enables signals from 64 transponders to be analyzed. During the tests, the visual information is displayed on an ordinary color television. Test data are printed in digital and graphic form on paper. One such instrument currently costs about 250,000 dollars on the world market. And there are buyers, to enhance labor productivity. Speeding up work is more valuable than money.

The data bank plays a major role in any modern automation system. A laser archive memory has been created at the Institute of Automation and Electrometry for permanent data storage. Imagine a carousel, set vertically with plates of 70x70 mm. In each one are holographically written 6,000 pages of text. The 288 plates forming the "carousel" can replace an entire book depository. The "catalog" is in the minicomputer, which controls the work of this data bank. Upon request, it chooses the necessary plate, covered with dark spots in which the archive information is coded. It then extracts it for illumination. The laser beam, lighting up the plate, reproduces the text and graphic image from the points.

The difference between the laser library and an ordinary one is that the text is reproduced on a TV screen. It can be read and extracted, and a printout or photocopy can be ordered from the screen.

In contrast to the magnetic memory, the laser one is resistant to electric and magnetic fields. Its range of use can be vast. The entire Lenin Library can be held in one room! The first to be converted to the laser memory will be scientific-technical and patent libraries, and sectoral data banks. Storage of design and engineering documentation, standardization services, space research files and law enforcement: these are but some of the areas where laser permanent memories will be used.

The institute is currently debugging the first industrial prototype of the laser memory, in conjunction with the Novosibirsk Instrument Building Plant.

But cooperation with industry is not always so successful. For instance, the plotter-coder mentioned above can draw 1.5-2 meters/second. It was created back in 1978.

A special interdepartment commission has noted its value for fast rough drawings. It is three times as productive as any similar system currently available and can be widely utilized, but is not yet in serial production. Many people come and ask how to acquire it. But the institute is not a factory.

Finally, enthusiastic supporters appeared, who undertook its production: one of the sectoral special design bureaus. But then the order was given to shift development to a system of standards in effect within the department. The bureau has been working on this alone for a year and a half already. Meanwhile, the CAMAC standard became an All-Union State Standard (GOST) in 1979.

Unfortunately, the CAMAC is still having difficulty making headway in industrial ministries. Each of them has its own standard for electronic equipment. To switch from the track of one agency to that of another, the "wheels" must be changed, as with trains crossing our border. But we're talking here about ministries that are within our country. Changing wheels takes a couple of hours, but switching from one standard to another takes years. Moreover, many ministries often create one-time automation systems for individual projects, to solve specific problems, not standard ones on the block principle as can be done by the CAMAC standard.

The June (1983) Plenum of the CPSU Central Committee emphasized that a uniform scientific and technical policy is now of decisive importance. Obviously, the "track" must be the same for all automation designers.

By some estimates, about one-sixth of all increases in labor productivity in the world is achieved by using computers. Scientific organizations actively working on creating such systems are thus particularly valuable. And it is important to create the conditions for developing their initiative and enterprise. Unfortunately, the tremendous intellectual capabilities of the academic institutes working in this field are still underutilized.

"We are constantly trying to get closer to production, to obtain a main outlet to industry", states academician Nesterikhin. "Two interdepartmental design sections were created for this in the industrial sectors ten years ago. We provided our people, and helped establish these sections. But they very quickly lost their interdepartmental nature and began to work on purely sectoral problems. One simply turned into a sectoral institute. We continue to cooperate with them, but now production has moved one barrier further from us.

Our situation is this: according to its budget (which barely suffices for salaries) and contracts, the institute does about several million rubles worth of scientific research work per year. The special design bureau of scientific instrument building of our Siberian division is doing about a million rubles worth of documentation for us. Yet a pilot plant is making finished devices for the institute for only 80,000 rubles!

We need to allow a scientific and technical association to be created as an experiment. The special design bureau of scientific instrument building must be completely subordinate to the institute (we now handle only scientific direction), and facilities provided for producing small series of automated systems. We could then offer sectoral institutes and industry finished, tested models for general serial introduction."

The situation of the Institute of Automation and Electrometry is typical for the Academy of Sciences. If one looks at the entire chain of academic institutes:

science, design bureau, pilot production, it is a pyramid tapering sharply upward. Only with such essentially scientific and technical firms as the Institute of Electric Welding imeni Paton of the UkSSR Academy of Sciences, which is making a major contribution to the development of the national economy, does this "pyramid" look normal: besides the design bureau, there are three plants.But the institutes of the Novosibirsk scientific center are all joined to only one pilot plant: a clearly abnormal situation. It is a body in which the head (science) is overdeveloped; the trunk (design bureaus) is very narrow, and the legs (production) are scrawny. But institutes, like people, must be well-balanced.

The recently adopted decree of the CPSU Central Committee and USSR Council of Ministers "Measures to Speed up Scientific and Technical Progress in the National Economy" calls for the rapid creation and outfitting of pilot and experimental bases and plants. Obviously, this must above all involve teams working in the most modern and promising directions of scientific and technical progress.

The Institute of Automation and Electrometry has a large number of very interesting, important projects awaiting realization. Under one roof is assembled technology that is divided among many sectors in industry. There are the energy and desire to be useful to the country now, today, not tomorrow. The USSR State Committee for Science and Technology must support the institute's initiative,aid in creating a scientific and technical association. This will speed up the automation process in many sectors of the national economy.

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MICROCOMPUTERS IN THE SHOP

Moscow IZVESTIYA in Russian 14 Oct 83 p 2

[Article by A. Romanov, deputy director of the USSR State Committee for Science and Technology, "Microcomputers Enter the Shop"]

[Text] The decree of the CPSU Central Committee and USSR Council of Ministers "Measures to Speed up Scientific and Technical Progress in the National Economy" emphasizes that extensive automation of technological processes is one of the main directions of work to accelerate scientific and technical progress. A key role in solving these tasks belongs to microprocessor technology. Its appearance in production signifies a new stage in the scientific and technical revolution. It is creating a qualitatively new basis for comprehensive automation of machinery, equipment and production processes.

What does a microprocessor look like? Imagine a semiconductor chip several square millimeters in size. The achievements of microelectronic technology allow an extremely complex circuit to be located in it: the main unit of a miniature computer, performing hundreds of thousands, and even millions of operations per second. Several more such chips form a main memory of hundreds of thousands of machine words. By combining such microcircuits with data input and output devices, we obtain the microcomputer, capable of solving extremely complex control problems. It is considerably less expensive than computer equipment used previously.

These advantages of microprocessors have defined the two major areas of their use. The first is to build microprocessors into machine tools, engines, robots and household items. By solving rather complex problems of program or optimal control, microprocessors greatly improve the technical and economic characteristics of those items in which they are installed. The second area is the use of microcomputers to control interconnected technological complexes, flexible adjustable processes, and automated enterprises.

Accumulated scientific experience and the considerable scientific "stockpile" show that extensive introduction of computers, especially microprocessors, into control of technological processes and equipment is a highly effective way of raising labor productivity and conserving labor, fuel and energy.

An economic analysis shows that the maximum effect per ruble spent is obtained not from individually used automation resources, involving isolated links in the production process, but comprehensive automation, encompassing all stages of production: from the arrival of raw materials to shipment of the final product.

These problems are especially acute in the machine building sectors. An important step was the creation of machine tools with numerical program control (NPC). Their efficiency rises considerably when microprocessor technology is used, along with robot manipulators. If machine tools with NPC, robots, transport equipment and automatic warehouses are joined into a single automated technological system, the economic return of the system is raised by a factor of several times.

The basic sectors of machine building, especially those requiring quick change of production, will switch to flexible, adjustable automated production processes in the near future. The basic control tasks of such processes will be solved by distributed microprocessor systems. They provide flexibility of the production complex given changes in the product mix. Additional capital expenditures are not required; one need only change the programs for the control system.

However, building such systems requires solving technical and organizational problems, one of which is a high degree of compatibility of microprocessor equipment.

Specialists know that it is difficult to create production control systems, and even those for individual assemblies, out of different equipment that can't be interconnected. Compatability of microprocessor components, various peripheral devices and automation instruments and tools must be standardized at the national level in the near future.

Program compatibility of microprocessor software must likewise be ensured. This requires standardization of sets of machine instructions, a single internal language for microcomputers and programming languages for control computers.

It will also be important in the future to have a single standardization program in the microprocessor area for the CEMA member countries. Figuratively speaking, microprocessors can only "understand" each other through standardized software, through uniform complexes of application programs. Development of international trade in products containing microprocessors will also be largely determined by the correlation between our microprocessor technology and international standards. Goods from the socialist countries using these resources will enjoy a higher demand if microprocessors can speak in the same "language" as their foreign colleagues. Firms in service maintenance of machines, automobiles and other goods in their countries will then be interested in buying and servicing the products of the socialist countries as well.

For the microprocessor to be reliable and inexpensive, it must have relatively simple computational possibilities: small word length, low main memory size, etc. But in this case programming will be more difficult, requiring more ingenuity and professionalism than for other computer types. Software development costs can thus be quite substantial.

Work must soon be organized to improve and disseminate acquired software to leading sectoral organizations responsible for introduction of microcomputers. This must be done based on the existing personnel in sectoral ministries, the USSR Academy of Sciences and higher schools. Without the creation and development of a software industry, we will be unable to avoid the costs of time and manpower for multiple replication of program creation for microcomputers in different sectors.

Another basic organizational question arises here: which ministries should create control systems based on microprocessors?

Back when automation was just beginning to get off the ground, control systems were created and distributed by only a few ministries, namely Minpribor. The extremely broad use of microprocessors requires a change in this conventional approach. If a rolling mill is built, its control system and software should be provided by the team that developed the mill. If it is a vehicle, then they should be generated by the vehicle designers, since no one can say better than they which problems the microprocessor must solve, and what role it must play.

Minpribor, Minradioprom [Ministry of the Radio Industry], Minpromsvyazi [Ministry of the Communications Equipment Industry], and Minelektronprom [Ministry of the Electronics Industry] for their part, must constantly expand the output of a clearly defined range of mass production, reliable spare parts, peripheral devices, equipment, instruments and microcomputers. Their availability will then be ensured through large scale production and relatively low cost. Only this will guarantee success in the complex, multifaceted work to automate production based on microprocessor technology.

Last but not least, there is the problem of training and retraining specialists. Those working in traditional fields in technology and engineering do not always accept new ideas and new technical solutions right away. To some extent, that has been the case with microprocessors. Many sectors have been unprepared for their general use because of a severe lack of specialists capable of handling the new technology.

To overcome the existing psychological barrier, the work facing us must be thoroughly examined. After all, we are talking about technology that is penetrating all types of machines, equipment, instruments and industrial complexes, including washing machines, household electric appliances and children's toys. In the near future, microcomputers, personal computers and microprocessors will be increasingly used as teaching aids and means for automating design, construction, office and other work. But this requires qualified specialists above all else.

USSR Minvuz, USSR Gosprofobr [State Committee for Vocational and Technical Education], and USSR Minpros [Ministry of Education], together with the State Committee for Science and Technology, USSR Academy of Sciences and the sectoral ministries must review the entire range of issues in personnel training and retraining. Programs are needed for schools and professional technical institutes of various types for teaching basic programming on the simplest microcalculators, microcomputers and microprocessors. Engineering students should master work on personal computers starting with their first courses. At higher level courses and in sectoral institutes for raising skills, engineers should possess solid programming skills in standard machine languages.

The leader in developing control systems based on microprocessors is the systems programmer, without whom highly efficient systems cannot be created. Specialists in automation and control systems should be taught the art of systems programming.

Of course, efficient training requires that academic institutions be equipped with standard stations and work sites for microcomputer programming and debugging. Soviet industry can provide them with the required equipment in the amount needed. All that is needed are perseverance and initiative from the above-mentioned ministries, and attention of planning and financial organizations to their needs.

Our country is working on the utilization of microprocessors in the national economy in close cooperation with the CEMA member countries. The industry of the Soviet Union and fraternal nations already produce high quality microprocessor equipment, in ranges and amounts sufficient for their general use in the national economy. Work is under way to create software for computer and control systems.

The active, purposeful work of scientific and production teams and design and industrial organizations, and attention of directors of ministries and departments, Party committees and Soviet organs will undoubtedly yield a successful resolution of the problem of general use of microprocessor technology for further intensifying and raising the efficiency of social production in sectors of the national economy, for fulfilling the tasks posed by our country's Central Committee.

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AUTONOMOUS MICROPROCESSOR CONTROLLERS FOR SCIENTIFIC RESEARCH AUTOMATION SYSTEMS

Leningrad IZVESTIYA VYSSHIKH UCHEBNYKH ZAVEDENIY: PRIBOROSTROYENIYE in Russian No 9, Sep 83 pp 61-66

[Article by A. B. Artamonov, L. K. Golovina, A. N. Zharikov, A. Kh. Mursayev, A. M. Smirnov and Ye. P. Ugryumov, Leningrad Electrotechnical Institute imeni V. I. Ul'yanov (Lenin)]

[Text] The microprocessor controllers of information measuring systems are considered. The block diagrams are described and the operating characteristics of the CAMAC crate controller, based on microcircuits of sets K580, K589 and micropower controllers based on microprocessor sets K587 and K588, are presented.

The level of development of microprocessor equipment now permits one to do away with minicomputers in experiment control or gathering of measuring data, having entrusted its functions to autonomous controllers made in the standard adopted for the system.

The CAMAC standard, widely used in scientific research automation systems, assumes organization of a system of individual functional units through a crate bus, or organization of a chassis controlled by a controller. In the case of autonomous use of a crate, the crate controller performs the function of control microcomputer, implementing the measuring data gathering and processing program [1, 2].

Specific limitations on the operating characteristics of the functional units and primarily on their economy are typical for portable autonomous information measuring systems. The restriction on consumed power in the range of 300-500 mW forces the designer of the systems to use BIS [large-scale integrated circuit] KMOP [complementary metal oxide semiconductor]. These series in Soviet industry are microprocessor sets of series K587 and K588.

Three microprocessor controllers of data gathering and processing systems are described in the article: the crate-CAMAC-VECTOR controller, realized on large-scale integrated circuit microrprocessors of sets of series K580 and K589 and two controllers for the field information measuring system realized on microcircuits of series K587 and K588.

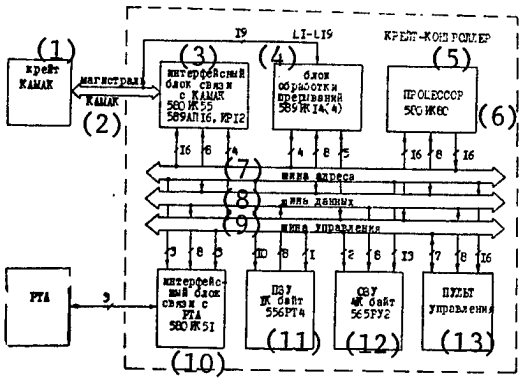

Figure 1. CAMAC-VECTOR Crate Controller

Key:

1. CAMAC crate
2. CAMAC bus
3. Interface unit for communication with CAMAC 580IK55, 589AP16 and IR12
4. Interrupt processing unit 589IK14 (4)
5. Crate controller
6. Processor 580IK80
7. Address bus
8. Data bus
9. Control bus
10. Interface unit for communication with PTA580IK51
11. ROM of 1 Kbyte 556RT4
12. Main memory of 4 Kbyte 565RU2
13. Control console

1. The CAMAC crate controller. A block diagram of the controller is presented in Figure 1. The crate controller is located on four standard cards and occupies four crate stations in which the processor, crate bus and teletype integration units, control console and memory (main memory of 4 Kbyte and ROM of 1 Kbyte), respectively, are located. The component base of the controller are large-scale integrated circuit microprocessors of sets K580 and K589 and integrated circuits of series 155, 565 (main memory) and 556 (ROM). The main characteristics of the controller are: time required to perform elementary operations (read from the main memory, write and logic operations) is on the order of 10 μs, the instruction time for data exchange in the CAMAC bus is 80-150 μs, the response time to an inquiry from the system unit is 270 μs, the consumed power with a control console is 25 W and data can be exchanged and the controller can be controlled either from an RTA-7B teletype or from the control console.

An addressing system, called mapping, in which the peripheral devices are addressed as memory cells, is used in the crate controller. The structure of the units for shaping the signals for controlling the reception and output of data from peripheral devices is simplified during mapping and it becomes possible to exchange data directly between the ROM and the peripheral devices,

due to which programs are shortened and the time of executing them is reduced and indirect addressing to the peripheral devices is simpler to organize. The address zone is distributed in the following manner: ROM and main memory addresses from zero, peripheral device addresses from 32K and CAMAC addresses from 48K. The ROM in the address field occupies the first kilobyte, which is determined by the characteristic feature of the design of the TsPE [expansion unknown]--the processor is addressed by hardware to memory cells 0,8,...,56 upon the occurrence of an interrupt. A total of the last 256 memory cells in the fifth kilobyte is allocated to the stack and if the address does not correspond to this zone when performing the stack write operation, an interrupt signal occurs.

Interrupt inquiries are distributed by priority in the following manner: the initial load program, three levels of program interrupts to support starting of programs, stopping and implementation of the instruction by instruction mode, interrupt from the teletype, NO-X interrupt and interrupt due to overflow of the stack and interrupt upon request of individual units of the system. The priority interrupt unit, which processes interrupt requests from the crate stations, is realized on three K589IK14 microcircuits and provides three service disciplines: priority in order of increasing the station number, group priority when interrupt requests are combined into three groups and each of them is assigned its own priority and a third mode--the absence of priority interrupts.

The CAMAC 24-bit word read and write registers are realized on a K580IK55 parallel peripheral adapter and three K589IR12 multimode buffer register circuits, respectively. The processor communicates with the teletype through the K580IK51 sequential peripheral adapter and the exchange is made at a speed of 50 baud. The control console is designed mainly to debug the crate controller and to find and correct malfunctions; therefore, it can be made in the form of a separate unit (station) and can be connected if needed. The control console performs the following functions: organization of direct access to the memory, starting the initial loading program, provision of program fulfillment in the loop mode, display of the contents of the address and data buses and also of the presence of signals I and Z of the CAMAC bus and hardware display of I, C and Z signals. The controller software is a resident program monitor, which is oriented toward the use of the RTA-7B teletype and occupies 1 Kbyte of ROM and 60 byte of the main memory. Other peripheral input-output devices can be connected to the system through the crate stations. The monitor provides fulfillment of the following functions: input of a data array from papertape or a keyboard, output of an array to papertape or printer, starting of a program by a given address with assignment of an arbitrary number of stop points, stopping of a program, continuation of an interrupted program, the instruction mode of fulfilling a program, printout of the contents of the register of the central processor element, transfer of a data array from one region of the array to another, data output in decimal and 16-bit codes and finding one or two bytes located alongside in the main memory with given contents with printout of the found addresses.

2. The micropower controller based on the K587 set. The micropower controller includes an autonomous portable measuring system, also organized on the

bus-modular principle, and is realized on the microprocessor set K587, which is four compatible large-scale integrated circuits made by KMOP technology, which provides low consumed power and high noise stability. The instruction system of the Elektronika NTs-03 microcomputer used in the controller contains 190 instructions, separated by the operating code and type of addressing and is universal in nature. The architecture of the processor and controller as a whole is similar to that of the Elektronika NTs-03. A block diagram of the controller, consisting of a processor PR, ROM and BSM integration unit, which provides communication of the internal bus of the controller to the system bus, is presented in Figure 2. The processor includes an operating unit OB, interface unit and a control and synchronization unit BUS, joined by a 16-bit intraprocessor bus.

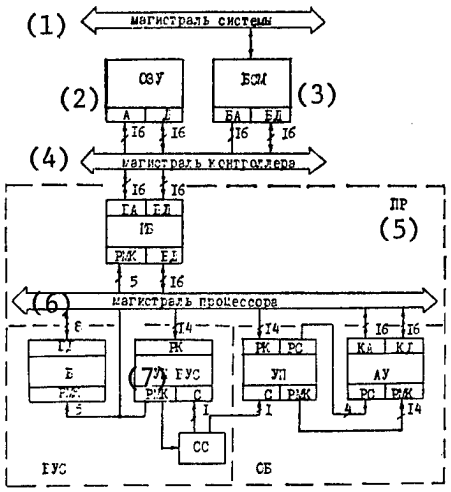

Figure 2. Structure of Micropower Controller Based on K587 Microprocessor Set

Key:

1. System bus
2. Main memory
3. Integration unit
4. Controller bus
5. Processor
6. Processor bus
7. Control and synchronization unit of control memory

The operating unit consists of a 16-bit arithmetic device AU and microprogram control memory UP and includes an internal processor bus with address channels KA and data channels KD and a 14-bit instruction register RK, a microinstruction bus and a bus that links the 4-bit status register of the arithmetic device to the status register of the control memory and that provides organization of branching in the conditional jump instructions. The operating unit is realized on four K587IK2 large-scale integrated circuits and 2 K587RP1 large-scale integrated circuits. The control and synchronization unit consists of a control memory UP BUS, buffer B and synchronization circuit SS. The UP BUS forms the microinstructions for control of data exchange between the processor units through the intraprocessor bus and provides initial starting of the processor and together with the synchronization circuit, synchronous servicing

of the instruction fulfillment process. The UP BUS is based on a single K587RP1 large-scale integrated circuit. The buffer B is designed to form and store operand addresses when executing instructions with different addressing methods and is based on a single K587IK1 large-scale integrated circuit. The synchronization circuit shapes the synchronization signal for the UP BUS and the signal of completion of instruction execution by the processor and the circuit is based on logic elements of series K564. The interface unit provides communication of the processor with the devices of the controller bus and is a data buffer based on two K587IK1 large-scale integrated circuits, which stores and transmits addresses and data.

The main memory consists of a storage device with capacity of 4K 16-bit words, operating control circuits and integration circuits with the internal bus. The working programs of the controller are stored on a cassette tape recorder, connected to the system bus through a communication interface unit, and are loaded into the memory by the initial loading program. The initial load is stored in the ROM with capacity of 20 16-bit words. Since Soviet industry does not produce micropower reprogrammable ROM, it is made in the form of a combination circuit based on medium-scale integrated microcircuits of series 564.

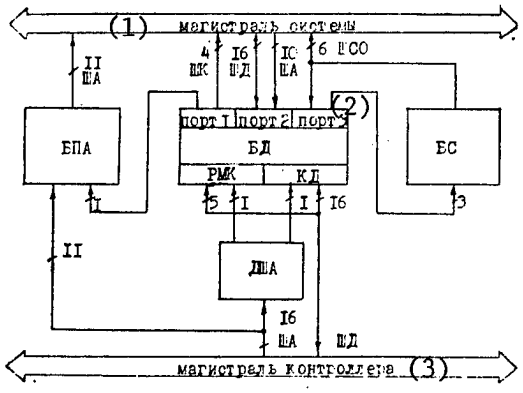

Figure 3. Bus Integration Unit

Key:
1. System bus
2. Port
3. Controller bus

The bus integration unit provides communication of the controller bus with the system bus. It consists of (Figure 3) an address decoder DshA, address transmission unit BPA, data buffer BD and synchronization unit BS. The integration unit is program-controlled. The data buffer has three input-output ports and is designed for instruction transmission by the functional units of the system, two-way data transmission, reception of interrupt source addresses, announcement signals from the units and shaping of synchronous exchange signals. The data buffer is based on two K587IK1 large-scale integrated circuits. The capability of program loading of the code to the microinstruction register of the data buffer is provided to control the direction of exchange. The address

transmission unit transmits address of the system units from the buffer of the interface unit of the processor to the system bus. The synchronization unit shapes the synchronizing signals during block transmissions of data from the functional units of the system to the controller. The address decoder, address transmission unit and synchronization unit are based on components of series K564. The general characteristics of the controller are speed on the order of 50,000 operations of the main memory-register type, operating time in the bus of 200 μs, dynamic consumed power of 1.0 W and hardware expenditures of 12 large-scale integrated circuits and 70 small-scale and medium-scale integrated circuits.

3. The micropower controller based on the K588 set. The most promising set for designing a micropower controller is the expanded microprocessor series K588, which includes a KR588VS2 arithmetic device, KR588VU2 control memory microcircuits, KR588VG1 systems controller, KR588IR1 micromode buffer register and KR588VA1 bus transceiver, now developed by industry. The use of an expanded set permits design of controllers with consumed power of 200 mW and speed of 200,000 short operations per second with operation time of 20 μs in the bus. The operating characteristics of the controller in the manufactured basic set are lower--speed on the order of 100,000 operations per second at consumed power of 250 mW. However, compared to the controller based on the K587 set, this version is more economical and is of independent interest.

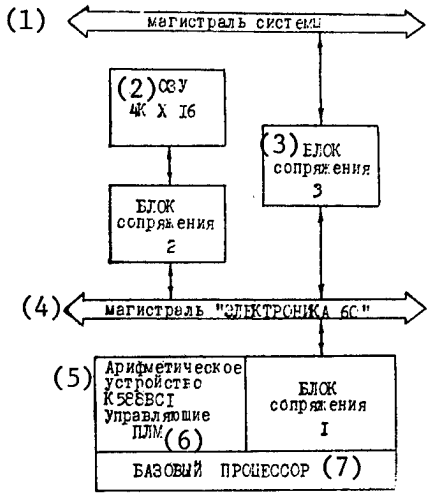

Figure 4. Structure of Controller Based on Microprocessor Set K588

Key:

1. System bus
2. Main memory
3. Integration unit
4. Elektronika-60 bus
5. K588VS1 arithmetic device
6. Control programmable logic arrays
7. Host processor

A consolidated block diagram of the controller is presented in Figure 4. The host processor consists of a 16-bit section of the K588VS1 arithmetic device, operating in the autonomous mode, and three K588VU1-003, K588VU1-004 and

K588VU1-005 control memory microcircuits in which the instruction microprograms of the Elektronika-60 microcomputer are written (the instruction system is abbreviated only in the part of conditional jump operations --up to four), and also in which the multiplication and division microprograms for 16-bit numbers are written. Conversion to the standard Elektronika-60 interface is accomplished by means of an integration unit realized on logic elements of the 564 series.

The integration unit with main memory, realized on static-type 537RU2 KMOP circuits with 4K X 1 organization, and an integration unit with system bus are also made on components of the 564 series. Since the microcircuits of the 588 and 537 series have TTL signal levels, the components of series 564 are also connected to a 5-volt power source. This also leads to reduction of the speed of the logic elements and of the controller as a whole, but reduces the need for level converters that consume considerable power. The hardware expenditures for realization of the integration units comprise 60 housings of the 564 series.

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MICROPROCESSORS FOR ANALOG SIGNAL PROCESSING

Leningrad IZVESTIYA VYSSHIKH UCHEBNYKH ZAVEDENIY: PRIBOROSTROYENIYE in Russian No 9, Sep 83 pp 67-71

[Article by V. B. Smolov, Ye. P. Ugryumov and I. V. Gerasimov, Leningrad Electrotechnical Institute imeni V. I. Ul'yanov (Lenin)]

[Text] The main problems of developing microprocessors for analog signal processing in integrated, modular and multicard versions are discussed. The results obtained at the Department of Computer Technology, Leningrad Electrotechnical Institute imeni V. I. Ul'yanov (Lenin), in development of software, hardware, programs, linguistic and methodical support of devices of this class are outlined.

Advances in the field of microelectronic technology, the desire to increase the technical operating indices of computer equipment and expansion of the class of problems advanced by science and practice have led to development of analog microprocessors (AMP). This term has been introduced by the largest American companies Intel and American Microsystems for the name of analog signal processing devices made in the form of one or several BIS [large-scale integrated circuit] and having the corresponding software and programs [1]. We shall expand this definition by introducing analog signal processing devices based on single or several cards containing a number of functionally complete modules.

Despite the considerable success in development of devices of this class both in the USSR and abroad, there is still a number of problems that require their own solution. A large volume of work on development of software, hardware, programs and linguistic and methodical support of analog microprocessors, which comprise one of the important classes of hybrid computers, is being conducted at the Department of Computer Technology, LETI imeni V. I. Ul'yanov (Lenin). The main results obtained at the department recently in development of analog microprocessors are outlined in the present article. The main problems of development of analog microprocessors include:

decomposition of analog microprocessors into functionally independent modules with maximum consideration of the capabilities of a given microelectronic technology from aspects of components and their hardware characteristics;

joining of functionally complete analog microprocessor modules into an integrated efficient computing structure that functions as a unit whole and equipped with the corresponding software and programs;

organization of effective interaction of parallel analog and sequential digital processors in combination with devices for conversion of the shape and type of signal display (analog-digital and digital-analog converters, pulse-width and pulse-frequency modulators and demodulators, voltage-current and current-voltage, voltage-charge and charge-voltage converters and so on);

an increase of the response of analog microprocessors under real-time operating conditions;

fulfillment of input-output data interface functions and necessary types of compatibility: program, code and time compatibility, by capacity between data sensors and the system in which the analog microprocessor is used as a structural element;

problem orientation of analog microprocessors by classes of problems to be solved;

provision of high-functional autonomy of analog microprocessors in combination with the capability of using them as the peripheral processors of measuring computer and control systems of different architecture;

development of all types of analog microprocessor support (software, hardware, programs, linguistic and methodical support);

development of firmware complexes for automation of analog microprocessor design.

The diagram shown in the figure reflects the basic directions of work of the Department of Computer Technology, LETI, in development of analog microprocessors. The design of an analog microprocessor is a complex integrated problem, successful solution of which is possible only with balanced development of all types of support. The analog microprocessor, being a generally analog-digital system, is difficult to subject to formal description, which determines the need to use multilevel mathematical models of analog microprocessors in different design stages: algorithmic, structural, functional-logic and technical. The variety of practical problems of analog signal processing requires the use of a wide range of mathematical linear (filtration, spectral analysis, correlation analysis and so on) and non-linear (linearization of the calibrated characteristics of different sensors, calculation of correction functions, data compression and so on) processing in combination with data gathering, storage and transmission functions. The hardware of analog microprocessors can be classified by different features, specifically:

by the type of application of analog microprocessors: systems-oriented and autonomous;

by the capability of restructuring: programmable in the instruction system, hardware restructurable and with rigidly defined functions (specialized);

by designation: debugging and built-in;

by the number of channels: single- and multichannel;

by the form of organizing the computing process: digital, programmable in the instruction system and functioning sequentially in time; digital, hardware-programmable and functioning parallel in time; analog, functioning parallel in time; and digital-analog, functioning sequentially-parallel in time;

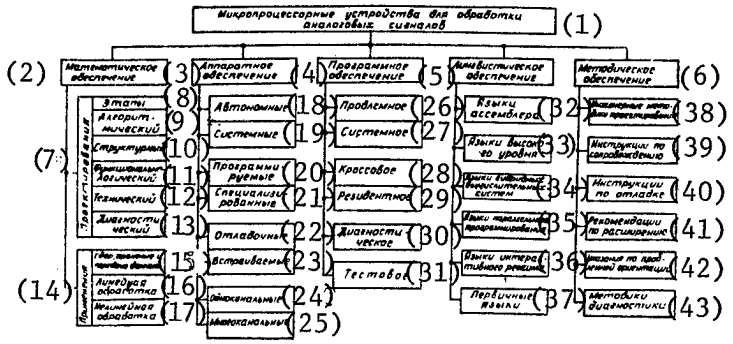
by the class of realizable functions: for linear or non-linear data processing, completion of gathering, conversion, storage and transmission functions of received equivalents of analog signals to upper levels of the system and so on;

by the design-technological version: integrated, hybrid (in the form of several BIS) and modular;

by the class of digital microprocessors used: with single-chip or sectional microprocessors;

by the component base--electronic based on different integrated circuit technologies and non-electronic;

by the form of display of the signals to be processed: homogeneous, without intermediate conversion and inhomogeneous, with intermediate conversion of the form of signal display



Key:

1. Microprocessors for analog signal processing
2. Software
3. Hardware
4. Programs
5. Linguistic support
6. Methodical support
7. Programming
8. Phases
9. Algorithmic

[Key continued on following page]

[key continued from preceding page]:

10. Structural
11. Functional-logic
12. Technical
13. Diagnostic
14. Applications
15. Data gathering, storage and transmission
16. Linear processing
17. Non-linear processing
18. Autonomous
19. Systems
20. Programmable
21. Specialized
22. Debugging
23. Built-in
24. Single-channel
25. Multichannel
26. Problem-oriented
27. Systems-oriented
28. Cross
29. Resident
30. Diagnostic
31. Test
32. Assembler languages
33. High-level languages
34. Hybrid computer languages
35. Parallel programming languages
36. Interactive languages
37. Primary languages
38. Engineering methods of design
39. Maintenance instructions
40. Debugging instructions
41. Expansion recommendations
42. Problem-orientation instructions
43. Diagnostic methods

We note that the use of programmable analog microprocessors that function sequentially in time is limited by their low speed. Moreover, far from each analog signal processing task permits sufficiently thorough parallel execution of the computing process, which would permit one to use multimicroprocessor systems. Due to the problem orientation of most measuring computer and control systems, the use of universal analog microprocessors is redundant. The latter results in an increase of the cost of both the hardware and especially of the programs. This circumstance determines the need for specialization of analog microprocessors by classes of problems to be solved, which is reflected directly in the nomenclature of the devices produced abroad for solution of typical analog signal processing problems. Analog (structured) methods of organizing the computing process are used in most analog microprocessors with rigidly defined functions: each operation is realized by a separate resolving element, all operations are executed in parallel and the connection circuit of the resolving elements is determined by the algorithm. Adjusting this device to the problem to be solved includes connection of the resolving elements according to the algorithm and assignment of the operating modes of the resolving elements [2, 3].

According to data from the literature, up to 90 percent of the cost of development of analog microprocessors, programmable in the instruction system, goes to development of programs. Unlike the fast reduction of the cost of hardware, the cost of programs decreases very slightly over time. Systems programs together with problem programs, determined by the specific designation of the analog microprocessor, form the internal programs of the analog microprocessor. The main function of the systems software is organization of the joint functioning of all structural components of the analog microprocessor. Moreover, its functions may include translation of user programs from external display to internal display in the machine codes of the microprocessor, loading and editing of programs, real-time automation of program debugging in a finished product, testing of microprocessor instructions, diagnosis of malfunctions, failure and error processing and various service functions.

When designing a specific analog microprocessor, one is usually limited by one or another complete set of systems programs. For example, there is no resident assembler in a problem-oriented analog microprocessor and it is desirable in a general-purpose analog microprocessor.

Problem programs are loaded into the systems medium by organization of the control program, the functions of which include: configuration of the resulting program according to user task from the problem programs modules, organization of the sequence of execution of autonomous programs, initialization of translation from the language of the applications program package, editing and transmission for execution, organization of data transmission between autonomous programs and support of supplementation and changing of problem modules. The control program is usually a set of catalogued procedures called in the order given by the user.

Much attention is being devoted in the department to implementation of measures directed toward reducing the cost of development of problem programs. The work is being carried out mainly in three directions: the first--duplication of programs of one type for a wide range of users, second--ever wider use of high-level languages. There are still many reserves on this route, since most programs for microprocessors are compiled in assembler-type languages, which of course have their own objective factors; the third direction --development and introduction of cross and resident debugging devices. The KAS-580/MOSK-580 cross system together with program complexes for automation of design procedures for simulation and analysis of hybrid computers AGUMS is now being operated successfully at the Department of Computer Technology, LETI, and at a number of industrial enterprises, which make it possible to reduce significantly the time and material expenditures for development of analog microprocessors. The cross system for programs debugging of a problem-oriented analog microprocessor, designed for autonomous application and solution of linear analog signal processing problems (the foreign prototype is the Intel-2920 analog microprocessor), is in the development stage.

The characteristic feature of linguistic support of the analog microprocessor is the presence of parallel programming languages in it and also of hybrid computer system (GVS) languages that include three groups of operators: analog, digital and hybrid. It is also planned to develop a set of programs designed for interactive development of an analog microprocessor and automatic compilation in the assembler language of the Intel-2920 analog microprocessor. Primary languages have been developed for a specialized type of analog microprocessor and are mainly employed in description of their structures in design procedures of simulation and analysis. An experimental prototype of a functional module (FM) for analog signal gathering and preliminary processing, based on a single-chip microprocessor of type K580IK80, has now been developed in the department. The functional module is designed for use in a measuring computer system having multilevel organization. The main functions of the functional module include:

programmable input of code equivalents of analog signals with wide dynamic range (60 dB) to a higher level processor of the system hierarchy;

linear processing of code equivalents of analog signals (digital filtration, scaling, averaging and so on);

non-linear processing of code equivalents of analog signals (calculation by given analytical functions, correction by calibration characteristics and so on);

checking the status of an entity, diagnosis of deviation of the operating mode from the norm in one or another format, localization of malfunctions in the system and so on.

Widespread introduction of microprocessors for analog signal processing will permit more complete and optimum use of the reserves for improving the main characteristics of measuring computer and control systems.

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OPTOELECTRONIC PROGRAMMABLE LOGIC ARRAYS

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 83
(manuscript received 18 Jun 82) pp 64-69

[Article by S. K. Li, E. A. Mnatsakanyan and V. I. Morozov (Moscow)]

[Text] Introduction. Despite LSI (large-scale integrated) circuit development being a major achievement in digital computer technology, the problem of diverse logic circuit production in small series remained unsolved since this entailed large inputs for LSI circuit design and production. To implement these logic circuits, programmable logic arrays (PLA's) have recently been developed and are being used more and more extensively in various computer hardware and digital automated machines. They are highly regular electronic logic circuits allowing computation of a set of specfic disjunctive normal forms (DNF) [1].

As a function of internal structure, PLA's are classified as those with combinatorial logic and those with memory [2]. Common to both is that they consist of two parts: The first part forms m conjunctions from n variables, and the second part forms l disjunctions from these conjunctions. They also have input and output buffers for translation into paraphase code or inverting input and output bits. The difference between these PLA types is that the PLA with memory has a p-bit feedback register between the second and first parts so that in this case $n = n_0 + p$ and $l = l_0 + p$ (n_0 is the number of external inputs, l_0 is number of outputs); the PLA with combinatorial logic has no feedback, i.e. $p = 0$.

Both PLA types can be both programmed one-time during manufacture or operation and reprogrammed by the user (the latter is henceforth designated RPLA). One of the main reasons the RPLA's have not yet been used extensively lies in the difficulty of rapid and "convenient" change in the type of DNF's implemented. Thus, for example, in one RPLA type, the contents are erased by ultraviolet or X-ray radiation for a half hour; after this, the electric method is used to reprogram it.

Thus, the main PLA characteristics (in addition to being reprogrammable) are time t, number of inputs n, outputs l and elementary conjunctions m. The values of these quantities for arrays in series production and described in the literature are [2]: $n \approx 10\text{-}20$, $m \lesssim 20$, $l \approx 50\text{-}100$ and $t \approx 30\text{-}250$ ns. The major advantages of PLA's in our view are high speed, parallel and multifunctional data processing and exceptional reliability since a malfunction often only produces insignificant reduction of n, l or m. It is evident that in reprogrammable structures, the latter two properties are considerably more pronounced. It is these properties that are most typical of processing in the optical range, which allows expecting the capability of developing rather fast optoelectronic RPLA's with brief reprogramming times.

Suggested in this work is the basic optical circuit for such a RPLA; its features are analyzed and some physical and geometric parameters of elements are evaluated. To avoid questions of effect and implementation of feedback between the two parts of the array, let us consider only the combinatorial type; the discussion below will also apply to the PLA with memory.

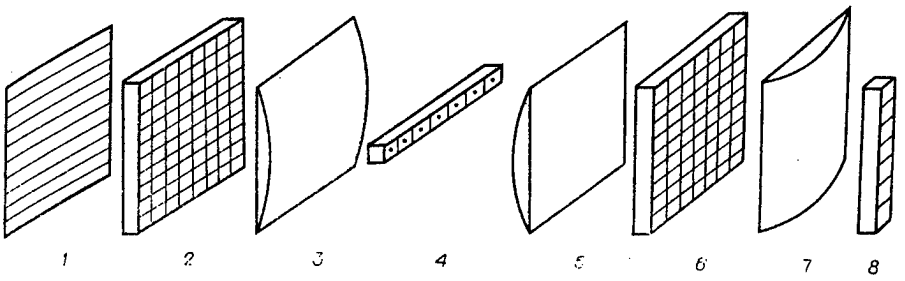

Fig. 1. Optical circuit for an optoelectronic PLA:

Key:

1. entry unit for binary variables in paraphase code
2. binary mask
3. cylindrical lens
4. row of photo detectors and emitters
5. cylindrical lens
6. binary mask
7. cylindrical lens
8. row of photo detectors

Basic Circuit for an Optoelectronic PLA and Its Functioning. Operation of the circuit shown in fig. 1 is based on optical methods of executing logic operations developed in [3]. Let a set of input variables $\{x_i\}$ be specified as a binary light pattern where each x_i corresponds to two horizontal bands: When $x_i = 1$, the first band is light and the second dark; when $x_i = 0$, the opposite is true, i.e. the variables are represented in paraphase code. This pattern is modulated by some binary mask, then converged in one coordinate (in this case, vertically) by the optical system with a cylindrical lens to a row of photo detectors, each of which is connected by the simplest logic circuit with its photo emitter (the latter also form a row). The logic

circuits must support switching the photo emitters on when there is no light on the corresponding photo detectors; in other words, inverting the optical signal coming into the input. Since the photo detector operates in this case as a threshold element and from the known formula,

$$\overline{a_1 \vee \bar{a}_2 \vee \ldots \vee a_i \vee \ldots \vee \bar{a}_{n-1} \vee a_n} = \\ = \bar{a}_1 \wedge a_2 \wedge \ldots \wedge \bar{a}_i \wedge \ldots \wedge a_{n-1} \wedge \bar{a}_n$$

(a_i is 0 or 1; $\vee$ and $\wedge$ are logical addition and multiplication), it is clear that the described part of the circuit implements a set of conjunctions of the type

$$k_1 = \bar{x}_1 x_2 \ldots \bar{x}_i \ldots \bar{x}_{n-1} x_n,$$
$$k_2 = x_1 \bar{x}_3 x_n,$$
$$\ldots\ldots\ldots\ldots$$
$$k_j = x_2 x_3 \bar{x}_n,$$
$$\ldots\ldots\ldots\ldots$$
$$k_{m-1} = x_5 x_6 x_7 x_{n-1},$$
$$k_m = \bar{x}_{n-1} x_{n-2} \bar{x}_{n-4} x_n.$$

Here m = the number of columns in the mask and thus the number of photo detectors. It is evident that type k_j is specified by the mask, for the presence or absence of x_i and $\bar{x}_i$ in this conjunction is fully governed by the corresponding cell in the mask.

The second part of the circuit is used to obtain l disjunctive normal forms from the computed conjunctions:

$$D_1 = k_1 \vee k_2 \vee \ldots \vee k_j \vee \ldots \vee k_{m-1} \vee k_m,$$
$$D_2 = k_2 \vee \ldots \vee k_{j-1} \vee k_{m-4},$$
$$\ldots\ldots\ldots\ldots\ldots\ldots$$
$$D_s = k_1 \vee k_3 \vee k_5,$$
$$\ldots\ldots\ldots\ldots\ldots\ldots$$
$$D_{l-1} = k_2 \vee k_4 \vee k_6 \vee k_8,$$
$$D_l = k_4 \vee k_5 \vee k_7.$$

The one-dimensional pattern from the row of photo emitters is converted by appropriate optics into a parallel beam consisting of vertical bands of light. Then this beam passes through the second mask and is again converged by the optical system (but now in the horizontal direction) to the row of photocells arranged vertically. Circuit output may be both electrical and optical. In

the latter case, the photodetectors have to be connected to the row of emitters, as in first part of system, but with no inversion of the signal from the photodetector.

Thus, the optical circuit shown in fig. 1 performs the functions of a combinatorial PLA. To make it reprogrammable, we have to replace the permanent masks by electrically controllable transparencies. This will allow, by changing control signals, generating any type of masks and thus changing the types of conjunctions and disjunctions. Reprogramming time will obviously depend on transparency type and format alone.

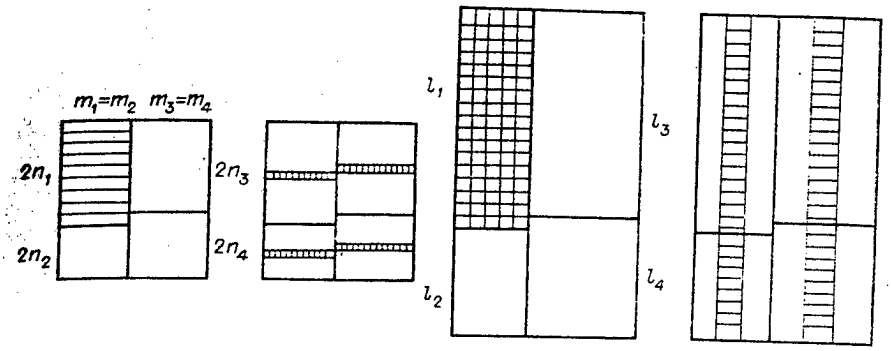

Fig. 2. Conversion of information in the optical circuit shown in fig. 1 for four optoelectronic RPLA's operating in parallel.

It should be mentioned that there is the possibility of implementing several optoelectronic RPLA's operating in parallel with two transparencies. Actually, when the information capacity of the transparencies is rather large, their working fields can be divided into sections, each of which performs functions of a variable mask in its optical channel. Shown in fig. 2 is the conversion of an input pattern as it passes through the optical circuit; the case when there are four RPLA's operating in parallel and independently is considered. From the drawing it is easy to understand the connection between transparency capacity, number of logic arrays implemented and their basic information characteristics. When the individual PLA's are arranged in one row,

$$N_1^1 = \sum_{i=1}^{I} m_i,\ N_2^1 = \max 2n_i,\ N_1^1 = N_1^2,\ N_2^2 = \max l_i,$$

where n_i, m_i and l_i are the i-th logic array parameters indicated above, and N^1_1 and N^1_2, N^2_1 and N^2_2 are the dimensions (in bits) horizontally and vertically of the first and second transparencies, respectively. But when the arrangement of the arrays is not uniform, the dimensions of the transparencies are governed by the number of rows and their maximal

length. Thus, for example, when $N^1_1 \times N^1_2 = 128 \times 128$ and $N^2_1 \times N^2_2 = 128 \times 256$ bits, implementation of 32 logic arrays arranged in four rows with the parameters $n_i = m_i = 16$, and $l_i = 64$ is possible.

Let us estimate the speed of response for this optical circuit. Ignoring the time for light passing through the circuit, we can assume that

$$t = t_1 + t_2, \text{ and } t_{1,2} = (t_{pho} + t_1 + t_e)_{1,2}.$$

Here, t is the speed of response for the entire circuit, t_1 and t_2 are the response times of the first and second rows of cells wherein t_1 and t_2 are made up of the response times for the photodetector t_{pho}, logic circuit t_1 and emitter t_e. Since the time characteristics of these individual elements are 10 ns or less, t may be 20-30 ns, which is comparable to the fastest electronic PLA's.

It is clear from this presentation that the characteristics of the transparencies do not affect the circuit response speed, but do fully govern reprogramming time. When both transparencies have standard row-by-row electric control and their control signals are changed at the same time, the time for reprogramming is

$$t_p = \max(\tau_i N_2^i),$$

where τ_i is the time for rewriting one row of the i-th transparency. Assuming $\tau_i \leq 10^{-5}$ s (which is quite achievable) and number of rows $N^i_2 \approx 2 \times 10^2$, we derive a value for t_p on the order of or less than 2×10^{-3} s. For uttrium orthoferrite transparencies, for which $\tau_i \approx 3 \times 10^{-8}$ s, reprogramming time is 10^{-5} s.

Analysis of Circuit Features and Evaluations of Some Characteristics of Its Elements. In the proposed optical circuit, both coherent and noncoherent light sources can be used as emitters. We think light-emitting diodes [LED's] are optimal for, on the one hand, they are suitable in dimensions and speed of response and are easily interfaced to electronics, while, on the other hand, operating in noncoherent light has a number of known advantages. Since the emission of each LED is divided only by m or 1 cells, it is easy to see that existing LED's and photodetectors fully meet these requirements [6].

From the viewpoint of estimated design, it is convenient to divide the circuit shown in fig. 1 into two parts, each of which can be considered separately. Since in the functional sense these parts are similar, it is sufficient to limit consideration to just one of them, for example, the first. Let light power P_{cell} be incident on the first cell of the transparency. The power of

the light converged by the cylindrical lens from all 2n cells in a column to the photodetector will be

$$P_{pho}(c) = \alpha P_{cell}[c + (2n - c)/K],$$

where α is the transparency transmission, c is the number of open cells in a column and K is contrast. To avoid false activations of photodetectors, $P_{pho}(1)/P_{pho}(0)$ must be >> 1 or K/2n must be >> 1 since only in this case can a photodetector threshold sensitivity be selected to confidently determine whether there is light in at least one cell in a column or that there are no illuminated cells at all.

As indicated in the introduction, $n \lesssim 20$; therefore the contrast must be $K \gtrsim 200$. In our view, electrically controllable transparencies made of liquid-crystal, magneto-optical and Seignette-electrical materials are the most promising for use in optoelectronic RPLA's. They have rather high contrast [5], but choosing them depends on the speed of response, working wavelength and other major characteristics required in the specific problem.

Read errors can also occur because of cross noise as a consequence of diffraction effects and aberrations of optical elements. Discussing aberrations is beyond the scope of this work; therefore, let us dwell just on evaluating the influence of diffraction effects in the case of noncoherent light. Noise on the i-th photodetector, evidently, is maximal when all cells in the i + 1-th and i - 1-th columns of the transparency are fully open. Thus, the spacing between the photodetectors (and thus between the columns) should be selected so that the intensity of the light incident on the i-th photodetector because of diffraction from the i + 1-th and i - 1-th columns, even in this extreme case, is considerably less than the intensity of one illuminated cell I_{cell}. Only then can one confidently determine the presence of at least one open cell in the i-th column against the noise background. To assess the required step in the row of photodetectors, let us use the known results of Fraunhofer diffraction, assuming for simplicity that the effective pupil of the optical system is circular. But in contrast to the conventional approach which considers only the size of the center spot in Airy's pattern, the secondary maximums should be considered here too. Actually, because of the imposition of diffraction patterns from 2n cells, the intensities of the maximums will increase 2n-fold and be comparable to I_{cell}. Therefore, the minimal step must be determined from the expression [7]

$$\Delta \approx (\lambda/d)2nrf,$$

where λ is the light wavelength, d is the diameter of the effective pupil, r is the ordinal number of the minimum of the diffraction pattern, and f is the focal distance of the optical system. From [7], it is clear that we can restrict ourselves to r = 4 and then, assuming $\lambda = 0.63 \times 10^{-6}$m, $n \approx 20$, $f = 5 \times 10^{-2}$m and $d = 3 \times 10^{-2}$m, we get $\Delta \approx 200$ microns.

Conclusion. The optoelectronic RPLA suggested in this work can have a high speed of response (about 20-30 ns) and brief reprogramming time (as brief as 10^{-4} - 10^{-5}s). The reprogramming procedure is very simple and essentially amounts to standard row-by-row switching of cells of electrically controllable transparencies. When transparency capacity is large, several RPLA's operating in parallel can be implemented with them. Considering what has been presented, we expect rather extensive application of optoelectronic logic arrays both in computer peripherals and central processors. They may be most promising where multifunction and parallel processing are required.

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METHOD OF ACCELERATION OF ARITHMETIC CALCULATIONS

Leningrad IZVESTIYA VYSSHIKH UCHEBNYKH ZAVEDENIY: PRIBOROSTROYENIYE in Russian No 9, Sep 83 pp 25-29

[Article by V. V. Barashenkov, O. G. Kokayev, V. G. Tarasov and T. E. Temirkhanov, Leningrad Electrotechnical Institute imeni V. I. Ul'yanov (Lenin)]

[Text] A method of accelerating multiplication and division operations, extraction of square root, binary-decimal conversions and calculation of elementary functions, performed by difference-iterative and the number by number method is considered. The procedure of finding the next smallest number, performed by hardware in a specialized homogeneous associative processor, is used as a means for elimination of excess iterations.

Number by number [1] and difference-iterative [2] methods of calculations are used extensively in design of specialized computer devices. The advantage of these methods is provision of high speed and accuracy of calculations with insignificant hardware expenditures. However, analysis of the utilized systems of recursion difference equations shows that they contain excess iterations--this is a reserve for an increase of speed. Those iterative loops (they can be called compensating) in which the main variables receive increments having opposite sign with respect to the initial increments are excess. It is suggested that the fast operation of finding the next lowest number in the reference array be used as a means to eliminate compensating iterations. The use of hardware realizations of the search procedures, described in [3], permits devices that realize the suggested method of calculations to be related to the class of associative processors.

Let us consider the use of the logic method of acceleration for completion of the multiplication-division operation U = zx/y. The iterative process in [2] suggests proceeding by the following algorithm:

$$\begin{aligned} x_{i+1} &= x_i + q_i \cdot x \cdot 2^{-(i+1)}, \\ y_{i+1} &= y_i + q_i \cdot y \cdot 2^{-(i+1)}, \\ \gamma_{i+1} &= \gamma_i - q_i \cdot y \cdot 2^{-(i+1)}, \end{aligned} \qquad q_i = \operatorname{sign} \gamma_i = \begin{cases} +1, & \text{if } \gamma_i > 0, \\ -1, & \text{if } \gamma_i < 0, \\ \text{stop}, & \text{if } \gamma_i = 0, \end{cases}$$

with initial conditions $x_0 = x$, $y_0 = y$, $\gamma_0 = z - y$, x, y, z are normalized binary fractions. The number of basic iterative loops is equal to the and size of independent variables n. During work of the algorithm, y approaches z and x approaches u. When using this operation to realize multiplication $u = z \cdot x$, the value of y is taken as equal to one. The initial value is $q_0 = -1$ and accordingly all iterations with positive increments can be eliminated. When using this operation to realize division $u = x/y$, the value of z is taken as equal to one, the initial value is $q_0 = +1$ and all iterations with negative increments can be eliminated. In the general case the modified algorithm of the multiplication-division operation looks as follows:

$$x_{k+1} = x_k + p \cdot x \cdot 2^{-t}, \tag{1}$$

$$y_{k+1} = y_k + p \cdot y \cdot 2^{-t}, \tag{2}$$

$$\gamma_{k+1} = \gamma_k - p \cdot y \cdot 2^{-t}, \tag{3}$$

where t is the minimum of the numbers smaller than n for which the condition $|\gamma_k| \geqslant y \cdot 2^{-t}$ is fulfilled. The desired value of t can be found by finding the next lowest among numbers $y \cdot 2^{-i}$ $(1 \leqslant i \leqslant n)$ with respect to the input symbol equal to $|\gamma_k|$. The initial conditions are: $x_0 = x$, $y_0 = y$, $\gamma_0 = z - y$, $p = \operatorname{sign} \gamma_0$.

The calculating procedure is completed when the input symbol $|\gamma_k|$ is less than or equal to the number $y \cdot 2^{-n}$ in the next loop. Since the number of iterative loops is variable, the average time of completing the operation must be used to estimate speed. The appearance of any binary combination is equally probable; therefore, the average number of loops is equal to (n + 2)/2. If the procedure of finding the next number is combined with calculation by formula (3), then the average time of the operation is

$$T = (n+2)\tau/2, \tag{4}$$

where $\tau = \max(\tau_{sl}, \tau_p)$, τ_{sl} is the time of performing the operation of adding two binary numbers and τ_p is the time of finding the next lowest number. When performing the restriction $\tau_{sl} \geq \tau_p$, we find the maximum twofold advantage in speed.

The use of the logic method of accelerating binary-decimal conversions and calculation of the square root is based on determination of the location of only single digits in the result code and the remaining digits are assumed zero digits. Some number z in the binary-decimal system of calculation is written in the form $z = \sum_{i=1}^{n} a_i p_i$, where $a_i \in \{0, 1\}$; $p_i \in \{\ldots, 0{,}1;\ 0{,}2;\ 0{,}4;\ 0{,}8;\ 1;\ 2;\ 4;\ 8;\ 10;\ 20, \ldots\}$ are the digit weights of the binary-decimal system, n^1 is the number of bits allocated to write the initial numbers, of which r digits are used to depict the fractional part and $(n' - r)$ digits are used to depict the whole part of the number. To convert the number from the binary system of calculation to the binary-decimal system, the following algorithm is suggested:

$$x_{k+1} = x_k - p_t, \quad z_{k+1} = z_k + 2^{n-t} \quad (a_t = 1), \tag{5}$$

where t is the minimum of the numbers less than n for which the condition $x_k \geq p_t$ is fulfilled and the values of p_t are located in the order of decrease, t = 1 corresponds to the maximum value, while t = n is the minimum value and n is the digit capacity of the output code. The initial conditions are: $x_1 = x$ is the initial number and all digits a_t of variable z are equal to zero. If $x_k < p_n$ when performing the next iteration, the result is formulated: variable z is equal to the desired binary-decimal number.

Example 1. The operation of an algorithm upon conversion of the number $21_{10} = 10101_2 \rightarrow 10\,0001_{2-10}$ is illustrated in Figure 1. The next smallest number with respect to x_1 = 10101 in the first loop is p_1 = 10100 and a one is written in digit a_1. The result is formed in the second loop after writing a one in a_6 at the location of variable z. Six iterations would be required to find the result without using the logic method of acceleration and four of them would be redundant. If the digit-weight references are selected from the set $p = \{\ldots, 2^{-2}, 2^{-1}, 1, 2, 4, 8, 16, 32, \ldots\}$ and if subtraction is carried out by the rules of the binary-decimal system, the numbers can be converted from the binary-decimal to the binary system by using the algorithm described by equations (5). The average time of binary-decimal transformations can also be calculated by formula (4).

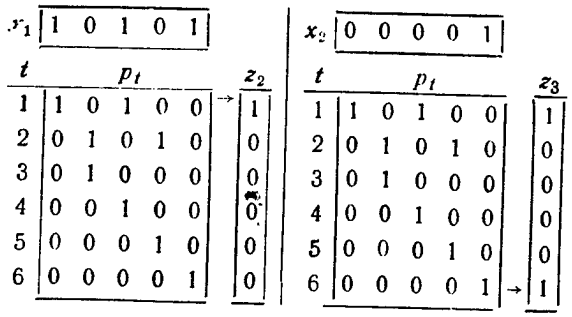

Figure 1.

Calculation of the square root is based on the use of the known relation:

$$(a_n + a_{n-1} + \ldots + a_i + \ldots + a_1)^2 = (a_n^2 + 2a_n a_{n-1} + a^2_{n-1} + \\ + \ldots + 2a_n a_i + 2a_{n-1} a_i + \ldots + 2a_{i+1} a_i + a_i^2 + \ldots + a_1^2),$$

where i varies from 1 to n and is the number of the bit of the result code, n is the number of bits in the result code and n is the number of the highest digit; $a_i = 2^i - 1$ is assumed to be processing of integers, but all arguments are also valid for numbers with non-zero fractional part. During operation of the algorithm, the numbers of those digits of the output code in which ones should be written are found sequentially, beginning with the highest digits. The initial number $x_1 = x$ is initially compared simultaneously with the values of a_i^2. The result of comparison will be the largest of the values of i for which $x_2 = x_1 - a_i^2 \geq 0$. The value of the output variable z increases by the value $a_i = 2^{i-1}$. The difference x_2 is compared in the second loop simultaneously with the values $2a_i a_j + a_j^2$ $(1 \leq j < i)$. The result of comparison will be the

largest of the values of j, for which $x_2 - 2a_i a_j - a_j^2 \geqslant 0$. The value of variable z increases by value $a_j = 2^{j-1}$. Calculation of the square root is completed if none of the differences $x_{k+1} = x_k - 2a_i a_m - 2a_j a_m - \ldots - a_m^2$ $(1 \leqslant m < \ldots < j < i)$ on the next k-th step is greater than or equal to zero. The algorithm is formally described by the following system of recursion difference equations:

$$x_{k+1} = x_k - z_k \cdot 2^t - 2^{2(t-1)},$$
$$z_{k+1} = z_k + 2^{t-1},$$

where t is the maximum of the numbers less than n for which the condition $x_k \geqslant z_k \cdot 2^t + 2^{2(t-1)}$ is fulfilled. The initial conditions are: $x_1 = x$, $z_1 = 0$.

Example 2. The operation of an algorithm in extracting the square root from the number $100_{10} = 1100100_2$ is illustrated in Figure 2. The arrow in Figure 2 shows the location of the reference which is the next least in the k-th loop with respect to the input symbol x_k.

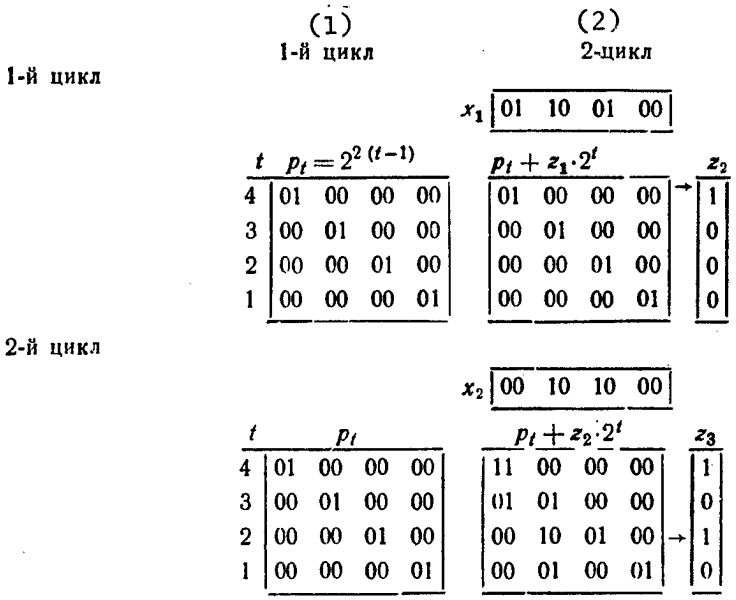

Figure 2.

Key:
1. First loop
2. Second loop

The speed of calculating the square root is estimated by the average time of performing the operation, which is determined by formula (4).

The Wolder algorithm [1, 2, 4] is used in calculating the values of the elementary functions. But because the length of the vector varies at each pseudorotation of it, one must keep in mind that exclusion of redundant iterations leads to a loss of accuracy of calculations; considerable additional expenditures of equipment are required to compensate for deformations of the length of the vector. Therefore, elimination of redundant iterations can be used only in calculation of functions not dependent on deformation of the vector: arctg z, arcctg z, Arth z and Arcth z; we will consider the algorithms for the first two of them in more detail.

The process of calculating the function γ = arctg z proceeds by the following algorithm:

$$x_i = x_{i-1} + y_{i-1} \cdot 2^{-t+1}, \tag{6}$$

$$y_i = y_{i-1} - x_{i-1} \cdot 2^{-t+1}, \tag{7}$$

$$\gamma_i = \gamma_{i-1} + \beta_t,$$

where t is the minimum of the numbers less than n for which the condition $y_{i-1} \geqslant x_{i-1} \cdot 2^{-t+1}$, $1 \leqslant t \leqslant n$ (n is the digit capacity of the output coat) and $\{\beta_t = \operatorname{arctg} 2^{-t+1}\}$ is the sequence of angular increments, is fulfilled. The initial conditions of the algorithm are: $x_0 = 1$, $y_0 = z$, $\gamma_0 = 0$. The calculations are completed when one of two conditions: 1) $y_{i-1} = x_{i-1} \cdot 2^{-t+1}$, 2) $y_{i-1} < x_{i-1} \cdot 2^{-n+1}$ are fulfilled in the next loop. The result will be the value of γ_i in the first case and the value of γ_{i-1} in the second case.

The algorithm for calculating the function γ = arcctg z is similar to the previous one:

$$x_i = x_{i-1} - y_{i-1} \cdot 2^{-t+1}, \tag{8}$$

$$y_i = y_{i-1} + x_{i+1} \cdot 2^{-t+1}, \tag{9}$$

$$\gamma_i = \gamma_{i-1} - \beta_t,$$

but the initial conditions ($x_0 = z$, $y_0 = 1$, $\gamma_0 = \pi/2$) and the stop conditions (1) $x_{i-1} = y_{i+1} \cdot 2^{-t+1}$; 2) $x_{i-1} < y_{i-1} \cdot 2^{-n+1}$)vary. If the procedure of finding the next lowest number is combined with calculations by formulas (6)-(7) and (8)-(9), the average time of calculating functions arctg z and arcctg z is one-half as much compared to performing these operations by the Wolder method.

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HIGH-PERFORMANCE SPECIALIZED PROCESSORS FOR CALCULATION OF ELEMENTARY AND SPECIAL FUNCTIONS

Leningrad IZVESTIYA VYSSHIKH UCHEBNYKH ZAVEDENIY: PRIBOROSTROYENIYE in Russian No 9, Sep 83 pp 30-34

[Article by V. B. Smolov, A. I. Vodyakho, V. U. Plyusnin and D. V. Puzankov, Leningrad Electrotechnical Institute imeni V. I. Ul'yanov (Lenin)]

[Text] Problems of design of specialized processors (SP) for calculation of elementary and special functions, oriented toward use in high-end models of YeS computers, are considered.

The basic requirement placed on specialized processors of this class is high calculation accuracy over a wide range at high speed. Number by number methods [1] or table-polynomial methods [2] are usually now employed in hardware realization of elementary functions (EF). The use of number by number methods is preferable for applications where the main requirement is minimization of hardware expenditures. Where the main requirement is to achieve high speed, preference is given to table-polynomial methods, since the latter permit variation of speed and hardware expenditures over a wide range [2].

A consolidated algorithm for calculation of elementary functions is presented in Figure 1. The calculation includes three main phases: preliminary processing, sampling of values of the expansion coefficient from the memory and calculation of the value of the polynomial and post processing. Preliminary processing includes reduction of the function to a narrow interval. Multiplications or reciprocal operations must be carried out for some functions. Preliminary processing also includes conversion of numbers from a floating-point format to a fixed-point format. In calculation of elementary functions with double accuracy, used in YeS computers (64 bits with floating point), calculation of a polynomial of fourth-fifth power is usually required. Post processing is required for some functions, which reduces to performing multiplication or addition operations [2].

Connection of the specialized processor as an arithmetic device with floating point is most effective when using a specialized processor for elementary functions in a computer system based on a high-performance general-purpose digital computer. One of the effective methods of increasing the efficiency

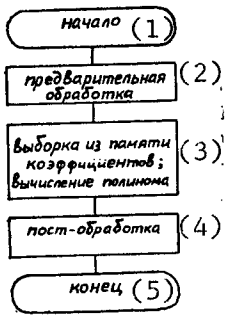

Figure 1

Key:

1. Beginning
2. Preliminary processing
3. Sampling of coefficients from memory; calculation of polynomial
4. Postprocessing
5. End

of the specialized processor is to expand its functional capabilities, which permits an increase of the utilization factor of the specialized processor equipment and a reduction of the volume of exchange with the baseline machine (BM). Three main sources of gaining an advantage in productivity (if one compares it to software realization) can be distinguished for specialized processors: hardware realization of elementary functions, hardware-microprogram realization of special functions and parallelling of the calculating process.

Depending on the method of achieving an advantage in productivity compared to the baseline machine, one can distinguish six types of specialized processors for calculation of elementary functions.

Processors of the first type are the simplest non-programmable specialized processors, for which the only source of achieving an advantage compared to software realization in the baseline machine is hardware realization of a limited set of elementary functions. The generalized structure of a processor of the first type is shown in Figure 2. The specialized processor includes three main units: a multifunctional adder-shifter (MFSD) that performs addition and subtraction operations with floating point and also preliminary processing, one or several high-speed multipliers (UMN), a tabular memory (PT) and a control device (UU).

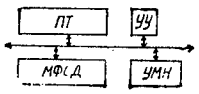

Figure 2

Processors of the second type are programmable specialized processors in which only main elementary functions (the baseline set) are realized by hardware and miscellaneous elementary functions and also special functions are realized by software or microprograms. The structure of a processor of second type is shown in Figure 3. Besides the adder-shifter, multiplier and tabular memory, the specialized processor includes a local register memory (MRP) for storage of intermediate results.

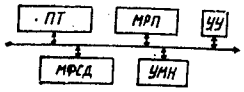

Figure 3

Processors of the third type are a system of specialized processors of type 1 or type 2, operating to a common tabular memory field. Processors of the third type are oriented toward use in microprocessor systems and are capable of simultaneous servicing of declarations coming from several instruction processors (PK). The common memory controller (KP) provides access to the multi-input tabular memory. If the stratification of the tabular memory is sufficiently deep, the time losses due to conflicts can be reduced to a relatively small value. The generalized structure of a processor of the third type is shown in Figure 4. The use of a specialized process of third type permits significant improvement of the technical and economic characteristics of the system, since hardware expenditures on the tabular memory comprise 30 to 70 percent of the total hardware expenditures in real specialized processors. Processors of the fourth type are distinguished from those of the third type by the presence of a common field of operating devices, which permits an increase of the load of the latter. Since hardware expenditures on the multiplier are considerably greater than on the adder, the use of multipliers as common resources is feasible. The generalized structure of specialized processors of fourth type is shown in Figure 5. The specialized processor includes n adders-shifters, a multi-input tabular memory, tabular memory controller, m multipliers (m < n) and switch (K). A time advantage can be gained in processors of the fourth type compared to software realization in the baseline machine not only due to hardware realization of the elementary function but also due to realization of the parallellism of adjacent operations [3].

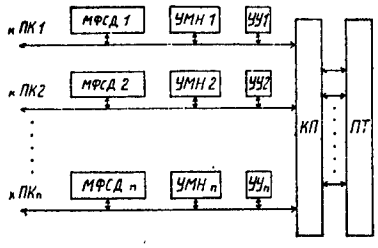

Figure 4

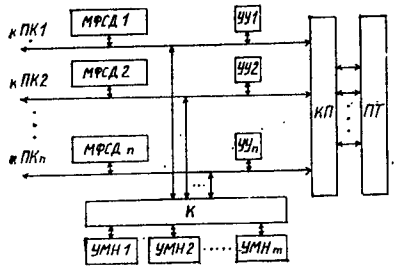

Figure 5

The individual multifunctional adder-shifter is separated from one instruction processor to service the declarations, while the tabular memory and the multipliers are used to service all declarations.

Processors of the fifth type are distinguished from those of the fourth type by the fact that none of the control devices has any arithmetic devices attached to them. The generalized structure of a processor of the fifth type is presented in Figure 6. The control devices that service declarations from the instruction processor operate to a unified field of arithmetic devices, which provides more efficient use of the resources of the arithmetic devices.

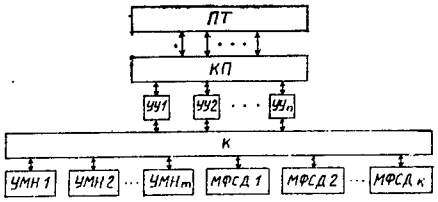

Figure 6

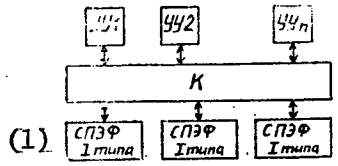

Figure 7

Key:
1. First type

Specialized elementary function processors of the first or second type, which can separate the common field of the tabular memory, are used as arithmetic modules in processors of the sixth type (Figure 7). Both single- and two-level organization of control can be used in SPEF [Special Processor of Elementary Functions]. The instruction coming from the instruction processor is interpreted by the microprogram with single-level organization. The use of the single-level principle of control is

feasible in processors of the first and second types. The use of two-level organization of control is feasible in more complex systems. The use of both synchronous and asynchronous control principles is possible at the instruction level. Two alternative approaches to selection of second-level operators are possible. The first approach assumes the use of operators for calculation of the basic elementary functions {sin, cos, ln, exp, arctg, $\sqrt{}$} and arithmetic operators {+, -, X, ÷} as the instructions. The second approach assumes selection of smaller operators. Such operators as reduction to an interval, conversion of their floating-point format to fixed-point format, sampling of their tabular memory and so on, can be distinguished along with operators {+, -, X, ÷}.

As shown by design experience, the use of SPEF of the second type, which on the one hand have sufficiently broad functional capabilities and on the other hand are sufficiently simple in internal organization, is the most effective for use in high-end models of YeS computers.

Let us consider as an example a specialized processor for calculation of elementary and special functions, oriented toward use in high-end models of YeS computers [4, 5]. The structure of the processor is shown in Figure 8. The specialized processor includes the following main units of the multifunctional adder-shifter: a multiplier-divider (UMD), registers-multiplexers M1 and M2, tabular memory and microprogram automation (MPA).

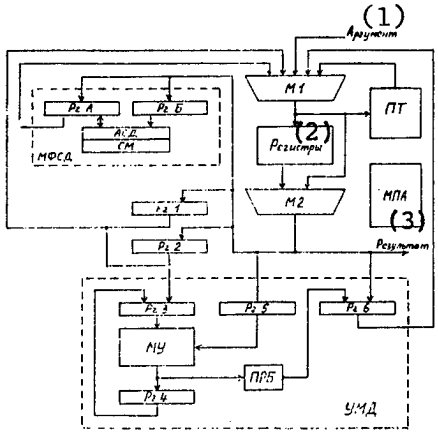

Figure 8

Key:
1. Independent variable
2. Registers
3. Result

The functions {e^x, ln x, $\sqrt{x}$, arctg x, sin x, cos x} are realized by hardware in the specialized processor. Miscellaneous functions are realized by hardware and microprograms. The table-polynomial method is used for calculations. A total of 1,024 sets of 64-bit coefficients is stored in the tabular memory for each of the functions. Each set includes five coefficients {a_0, a_1, a_2, a_4}. The values of the elementary functions are calculated by the Horner

scheme: $P(x)=((a_4x+a_3)x+a_2x+a_1)x+a_0$. Moreover, auxiliary tables used in calculation of functions e^x and ln x are stored in the memory.

Preliminary processing is performed on the multifunctional adder-shifter, which includes two registers (RgA and RgB), an adder SUM and a shifter, made on the basis of a multiplexer (ASD). The 10 highest digits of the independent variable reduced to the interval are used as the address of the tabular memory.

The UMD unit performs multiplication, division and inversion (1/x) operations. The structural and algorithmic solutions used in the UMD are oriented toward achievement of maximum speed in realization of multiplication, since the length of this operation is the determinant in the total time expenditures for calculation of elementary functions by the table-polynomial method. A matrix multiplier, operating in the sign-digit number system [6], comprises the basis of the UMD. The matrices contain two stages of sign-digit adders-calculators. Four digits are multiplied or four numbers of the quotient are found during one pass through the matrix. Auxiliary shift registers Rg1 and Rg2 are used in division for storage and shifts of the dividend, divisor and quotient. Besides a matrix multiplier, the UMD includes four registers Rg3, Rg4, Rg5 and Rg6 and a converter (PRB), which provides conversion from sign-digit to ordinary representation.

(1) № п.п.	(2) Функция	(3) $T_{ср}$, мкс
1	+	0,22
2	×	0,72
3	:	2,45
4	exp	4,8
5	ln	3,3
6	$\sqrt{X}$	3,3
7	arctg	4,5
8	sin (cos)	4,0

Key:
1. Number of item
2. Function
3. μs

The specialized processor includes a unit of 16 64-bit microprogram-accessible registers. Microprogram automation, the length of the loop of which is 72 nanoseconds, maintains control. The microprogram memory capacity is 2K 36-bit words. The processor is realized on an ESL of series IS-500 on standard designs of YeS computers. The time of performing basic arithmetic operations and hardware-realizable elementary functions is presented in the table.

The processor is designed for connection to the YeS 1065 as an arithmetic functional expander and provides a 7-10-fold time advantage in calculation of elementary functions compared to software realization.

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SYSTEM FOR RECORDING AND INPUT TO COMPUTER OF ONE-DIMENSIONAL IMAGES OF DIM OBJECTS AND HIGH-SPEED PROCESSES

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 83
(manuscript received 31 Dec 82) pp 3-7

[Article by Yu. V. Bondarenko, V. Ya. Budtsev and A. N. Kasperovich (Novosibirsk)]

[Text] The problem of recording optical images with brief duration and low intensity is relevant in the broad class of physical research of fast-flowing processes. Traditional photographic methods of recording an image from a screen of an electronic-optical converter, usually used to solve it, precludes the possibility of online monitoring and control over the course of a frequently expensive experiment, makes the procedure for input of the experiment data into a computer difficult and makes the processing of information processing lengthy and laborious [1].

To solve this problem, systems based on highly sensitive transmitting television ELT [CRT's] combined with special-purpose minicomputers have recently been developed. With the appropriate software, these systems are an efficient tool for image recording and processing. The known foreign systems in this class are [2-4]: OMA (Optical Multichannel Analiser), OSA (Optical Spectra Analysis) and MfR (Microcomputer for Research). There are reports of development of domestic laboratory systems, but such equipment is not being produced by industry. Therefore, development of this type of recorder with a domestic element base and research of its capabilities are relevant.

Shown in fig. 1 is a block diagram of a system developed for recording one-dimensional images. The system contains an image receiver, a focusing and deflecting system (FOS), a unit for standard television [TV] signals, a reading amplifier, unit for controlling CRT gun, digital processing unit, visualizer, control unit and high-voltage power supply for CRT section.

The system is supplied with a TV monitor which simplifies tuning of it and selecting a line for subsequent processing; it also allows tracking quality of the image being recorded and photographing it when necessary.

Used as the image receiver is the domestic LI-702 supervidicon (supersilicon) which is a transmitting CRT with a diode-mosaic silicon target [5]. With high

Key:

1. high-voltage unit
2. gun control unit
3. video signal
4. container
5. amplifier
6. control unit
7. keyboard
8. level matcher
9. 12-bit line counter
10. 8-bit frame counter
11. synchronizer
12. external sync pulse
13. external device start
14. TV monitor
15. raster
16. KTP-39 camera
17. digital unit
18. address generator
19. normalizing amplifier
20. 6-bit ADC
21. 512 x 6-bit storage
22. DAC
23. visualizer
24. CAMAC bus

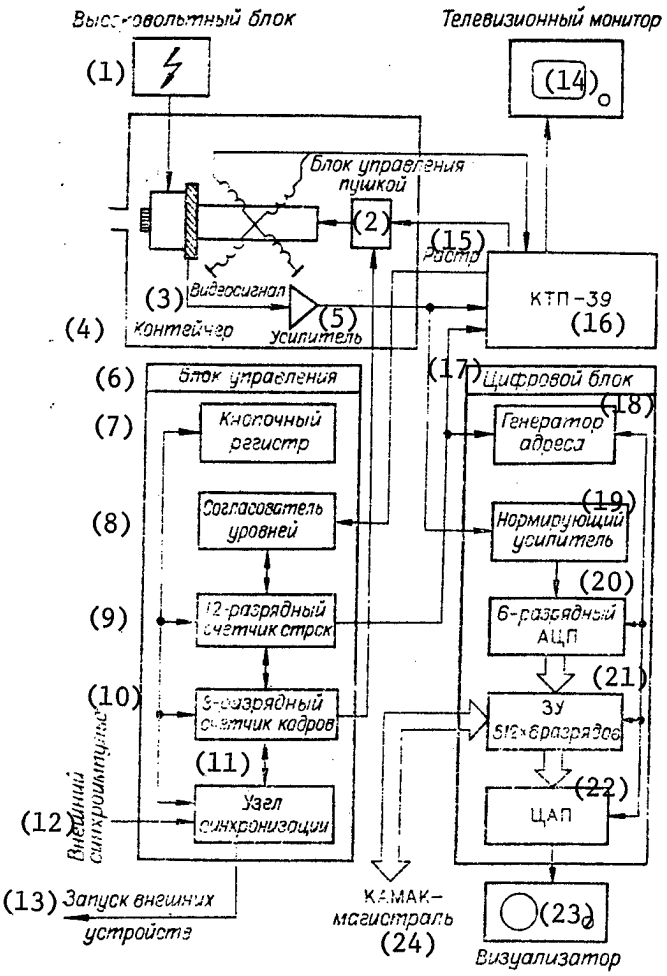

photo sensitivity, broad spectrum range, no photoelectric inertia, capability of storing an image on the target, the supervidicon is suitable both for recording of one-time short-duration processes and for analyzing stationary dim objects with the capability of storing an image on the target.

Fig. 1. One-dimensional image recorder

An image is read from the supervidicon in the standard TV mode, i.e. interlaced scanning of full frame with 625 lines at 25 Hz. Electric scan signals and voltage needed for supervidicon operation come from the KTP-39 camera without substantial redesign of the latter. Used as the supervidicon focusing and deflecting system is the FOS-10 for the same camera, in which the permanent magnet is replaced by a coil fed by a stabilized current source to improve focusing.

The CRT gun control unit is needed to blank the electron beam for the time of the reverse course. An electron key in the unit is controlled by a TV raster signal. The beam is controlled by varying the cathode potential with constant modulator voltage (in contrast to the modulator control method usually used). This allowed reducing control voltage size and target focusing. The control

unit blanks the beam when there is no line scan and thereby protects the target against burning. The capability of blanking the electron gun by external pulse for the time needed to store an image on the target is provided.

The target current is converted into electrical voltage with maximum amplitude of 1 V by a reading charge-sensitive amplifier with a 10-MHz bandwidth. The amplified video signal is fed through a cable to the input of the normalizing amplifier which matches the capacitive input resistance of the ATsP [analog-to-digital converter = ADC] to the cable and creates the bias needed for the converter. The amplifier is made with an operational amplifier circuit with discrete elements. Bandwidth is 10 MHz and gain factor is 1. The video signal simultaneously goes to the input of the KTP-39 video amplifier and is used to display the image on the monitor.

From the normalizing amplifier output, the video signal is fed to the ADC input. The high-speed 6-bit ADC is made with the 1107PA1A microcircuit and operates at a 10 MHz sampling rate which corresponds to 512 samples per line. This rate stemmed from the condition of identical vertical and horizontal resolution. Increasing the number of samples on a line makes sense only when the reading beam diameter is reduced.

The high rate of data arrival from the ADC does not allow direct recording of it in computer memory. Therefore, results from converting the video signal are recorded in high-speed storage implemented with 12 packages of K155RU5 microcircuits. The address generator forms a series of 8-bit words and the control strobes needed to operate the storage unit and ADC.

The K572PA1A digital-to-analog converter [DAC] is used to output information from the storage unit (profile of image intensity by selected line) to the visualizer, an oscillograph. The clock generator operates at 10 MHz in record, and about 25 kHz in regeneration mode.

The control unit, the controller, controls the majority of system units and synchronizes system operation with the process being investigated. The front panel on the controller contains control keys to specify the line number to be read (from 1 to 312), the number of fields, in the course of which an image is stored on the target (from 1 to 99), and the synchronization type (internal or external). The location of the line selected for processing relative to the full image is indicated by the monitor cursor. The controller has a converter for converting input TV signal levels to TTL levels, a 12-bit line counter and an 8-bit field counter. The controller generates the pulse with the specified width needed to blank the electronic beam while an image is being stored and the pulse for authorizing operation of the address generator.

The system operates like this. On a "Record" command generated from an external sync pulse or control key, the controller blanks the supervidicon reading beam. At the same time, the line number and number of fields are written from the external registers to the input registers for the respective counters. The address generator is stopped and reset to zero. At the trailing edge of the current pulse for the fields, the synchronization strobe which activates

the field counter is generated. This same pulse may be used to start external devices. The pulse output from this counter authorizes operation of the line counter. The latter at the specified line opens the electron gun and starts the address generator. As a result, the coded video signal of the line selected is written to storage. Also generated from the line counter command is a cursor pulse which is fed to the KTP-39 camera video path, after which the cursor indicating the location of line being processed appears on the monitor. At the end of a record cycle, the system is automatically switched to and remains in the regeneration mode until the next "Record" pulse arrives.

To reduce extraneous illumination and parasitic supervidicon pickup, the latter and the deflection system are housed in a lightproof container made of duralumin. Inside the container, the reading amplifier is very close to the target on the screen. The beam control unit and anode voltage filters board are near the CRT plug.

The high-voltage unit is made according to the well-known scheme containing a blocking oscillator, step-up transformer and three voltage multiplier units. Output voltage is regulated from -5 to -10 kV. The unit is made as a stand-alone unit and attached to the CRT container very close to the transfer unit.

In design, the controller and digital processing unit are made as two separate modules following the CAMAC standard. All needed connections are made through plugs on the front panel of the modules, container and KTP-39 unit.

The system was tested in the mode for recording high-speed processes and in the mode for storing an image on the supervidicon target. System spatial resolution did not deteriorate when exposure time was reduced to 100 ns. At room temperature, it is advisable to perform storage of an image on the target for 5-6 frames (about 200 ms). To have the capability of increasing storage time, the target should be cooled to reduce leakage current and thermal noise.

The system developed was used to analyze the spectrum composition of pulse radiation in an experiment on exciting a laser resonator with two mirrors that convert the wavefront (OVF-mirrors) [6]. In this experiment, usually the pulse pattern of inteference rings, the space between which characterizes the phenomenon under investigation, has to be photographed. This method of recording and subsequent processing of photographs slows down the experiment and makes it difficult to perform.

By using the system developed, the spectrum intensity profile after each laser burst was output to the oscillograph. This allowed quick tuning of the experimental apparatus, obtaining laser radiation with the specified spectral characteristics and studying the relation between the radiation spectrum and resonator parameters. Fig. 2 is the intensity profile for the radiation spectral semi-rings photographed from the system display screen. Fig. 3 is the images of the rings themselves photographed from the monitor screen. The lifetime of the individual components of the spectrum was about 5 ns and was monitored by an FEK [photoelectric colorimeter] detector and an I2-7 oscillograph.

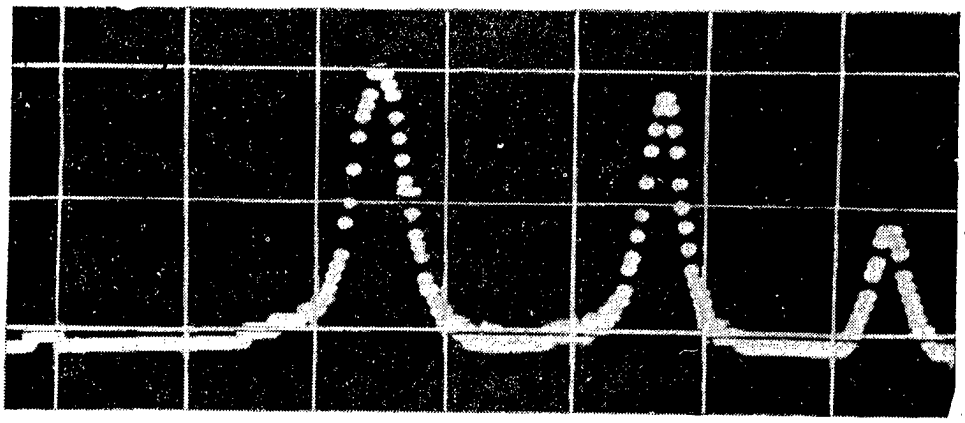

Fig. 2. Intensity profile for the radiation spectral semi-rings photographed from the system visualizer screen.

Fig. 3. Images of rings themselves photographed from the monitor screen.

System tests performed showed that it is simple to use, and the information output by it is clear and allows online adjustment of the course of the experiment.

Supplemented with relatively simple interface equipment, the system is easily interfaced to a minicomputer through the CAMAC bus. Along with software facilities, this system may become the base unit in systems for recording both one-time images and stationary processes with low intensity.

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METHODS FOR SOLVING PRINTED CIRCUIT BOARD DESIGN PROBLEMS WITH THE 15UT-4-017 INTERACTIVE GRAPHICS SYSTEM

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[Article by V. Ye. Mezhov (Voronezh)]

[Excerpts] Interactive 15UT-4-017 graphics system development enabled automating the most tedious stages in logic modeling, circuit engineering, and topological design of IC's and LSI circuits [1, 2]. Given in [2] are the main features of the software package for PCB design by using the 15UT-4-017. This work considers the language for describing the source data and dialogue and the main methods for solving PCB design problems with the 15UT-4-017 system.

Interactive language facilities used in PCB design with the 15UT-4-017 system include the source data description language (YaOID) and language for dialogue in the design process which are subsets of the YaZOS-U input language [3].

In the final stage of PCB design, the system enables obtaining control information for preparing PCB drawings on the EM-721, EM-732 and EMN-7022 plotters, for creating photo originals with the KPA-1200, EM-538 and other apparatus, and for automatic drilling and assembly of PCB's using NC machine tools with optimization of operating time.

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VALUATION OF A PROGRAMMER'S WORK

Moscow EKONOMICHESKAYA GAZETA in Russian No 36, Sep 83 p 7

[Letter from reader G. Pasternak-Taranushenko, economist, Kiev]

[Text] On 26 November 1982 the Ministry of the Automotive Industry approved a price list for integrated debugging of special software and nonstandardized hardware for automated process control systems (Ts 37.051.053-82); the price list takes the instruction as the unit measurement of work. Use of the price list is mandatory; it is a normative document.

However, anyone connected with programming knows that the more skilled a programmer is, the shorter the program he will write. Therefore, a price list that evaluates work according to the number of instructions in the program does not promote increased productivity and does not stimulate programmers to do better and more economical work.

It is quite obvious that the work of programmers could be better evaluated according to the number of functions reflected (encompassed) by the program. The significance of the functions should be taken into account. Of course, one must take a thoughtful approach to the issue of evaluating work and make use of statistical material.

12488
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UDC 681.3.021

SOFTWARE DEBUGGING DEVICES FOR MICROPROCESSORS

Leningrad IZVESTIYA VYSSHIKH UCHEBNYKH ZAVEDENIY: PRIBOROSTROYENIYE in Russian No 9, Sep 83 pp 53-61

[Article by P. P. Sypchuk, A. D. Ivannikov and I. D. Kurilovskiy, Kharkov Polytechnical Institute]

[Text] The classification of software debugging devices for microprocessors is presented. A program debugging system is considered for devices based on the K580IK80 microprocessor, which includes a cross system realized for the SM-4 computer, and an OKA-80 resident hardware-software complex. The composition of the hardware and software of the OKA-80 complex is described in detail and data organization for the KSI-1 cross system is presented. The resident and cross devices are described with analysis of their advantages and disadvantages with respect to design of hardware of various designation. Recommendations on applications are presented.

Microprocessors won a significant place from the first moment of their appearance in digital hardware of the most diverse purpose. The functional flexibility, high reliability, ease of design and capability of realizing complex control algorithms make it possible to use microprocessors not only to design hardware, which was earlier designed on the basis of small- and medium-integration logic IS [integrated circuit], but also make it possible to design systems with qualitatively new characteristics.

The main distinguishing feature of devices designed on the basis of microprocessors is transfer of the main weight of realizing the functional algorithm of the device to the software. The need to design large volumes of software and its strong dependence on the designation and configuration of the microprocessor led to the appearance of various types of devices for automation of development and debugging of programs for microprocessors. These devices can conditionally be divided into software, software-hardware and hardware-software.

Software includes program complexes written for universal computers, which include cross assemblers and cross compilers, an also debugging emulators.

The structures and algorithms of cross assemblers and cross compilers are similar to the structures and algorithms of assemblers and compilers developed for universal computers. The debugging emulators contain programs that simulate execution of instructions by the microprocessor and debugging programs that permit one to follow the course of simulating the execution of the program to be developed and to make changes in it. The wide range of peripheral devices and the developed operating systems of universal computers offer great capabilities to the developer and user of the design system: convenient methods of creation and management of libraries of programs to be debugged, standard debugging management devices, effective interaction of the user with the computer, the capability of simulation of situations, debugging of which is difficult on a real control object, and so on. The disadvantages of modern design systems on large and minicomputers are: the high cost of their use, the lack of capability to debug the hardware of a microprocessor, the lack of capability of joint debugging of software and hardware together with the controlled object in real time. These systems have found application mainly in development of software for microprocessor devices created on the basis of single- and multicard microcomputers having standard hardware [1].

Cross assemblers and cross compilers are also used in software-hardware systems to produce programs in microprocessor codes, but the microprocessor itself, operating under the control of a universal computer, is used to implement these programs. Having the advantages of software systems, software-hardware systems permit one to debug programs for microprocessors operating in real time, while the presence of intracircuit emulators in these systems offers the capability of debugging the hardware of the device to be developed. But these systems themselves are more complex since they require special hardware for joint operation of the universal computer and microprocessor. Moreover, they are usually developed on the basis of microcomputers that do not have such developed service software as large computers and do not free the user of the need to be familiar with two computer systems. Hardware-software represents microcomputers designed on the basis of the same microprocessor as the device to be developed and equipped with the necessary peripheral equipment and software for debugging of programs. The class of these systems is rather broad: from single-card estimator modules to complete hardware-software complexes that approach minicomputers in their characteristics [1]. Hardware-software systems provide parallel design and joint debugging of software and hardware of microprocessors. The capabilities of these sytems are determined by the memory capacity, the presence of an external memory, the set of peripheral devices and the composition of the systems software. The cost of hardware-software debugging complexes is determined mainly by the cost of the peripheral devices and is usually considerably lower than the cost of the minicomputer. Operation of these complexes is less expensive than that of universal computers. A trend toward preferred use of hardware-software debugging complexes has been observed in this regard with development of microprocessors.

Let us consider as an example of debugging devices the software development system for microprocessors, designed on the basis of the K580 microprocessor series (Figure 1). This system includes cross devices realized on the SM-4 computer and the OKA-80 hardware-software debugging complex.

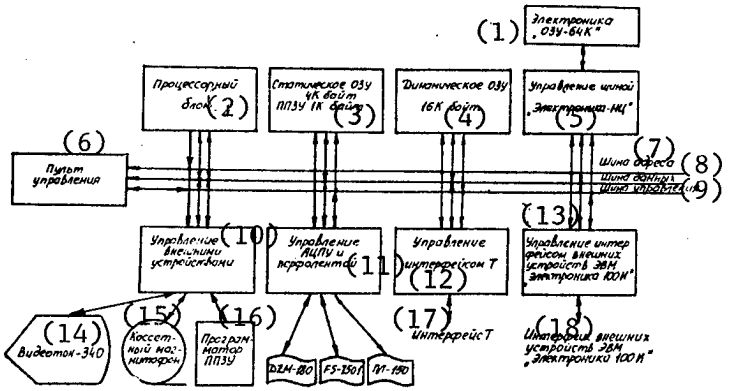

Figure 1. Configuration of Hardware of OKA-80 Hardware-Software Debugging Complex

Key:

1. Elektronika OZU-64K
2. Processor
3. 4 Kbyte static memory and 1 Kbyte PROM
4. 16 Kbyte dynamic memory
5. Control of Elektronika-NTs bus
6. Control console
7. Address bus
8. Data bus
9. Control bus
10. Peripheral device control
11. Alphanumeric printer and papertape control
12. Interface T control
13. Peripheral device interface control of Elektronika 100I
14. Videoton-340
15. Cassette recorder
16. PROM programmer
17. Interface T
18. Peripheral device interface of Elektronika 100I computer

A number of solutions used in the MIKRO-80 complex are employed in the OKA-80 hardware-software complex [2]. Its hardware includes:

a central processor module designed on the K580IK80 microprocessor using microcircuits of series K589 and K155. The module contains a step program execution circuit and interrupt signal response circuit when executing instruction of the user program, which are employed in program debugging. These circuits include toggle switches located on the front panel of the module. The display of signals in the address bus, data bus and control bus is also brought out to this panel;

the memory module, containing a static type main memory with capacity of 4 Kbyte based on K565RU2 microcircuits and a plug for installation of a PROM with capacity of 1 Kbyte, designed to store the control monitor. A toggle switch for switching off the PROM and interlocking the main memory is located on the front panel of this module;

a dynamic main memory module with capacity of 16 Kbyte, designed on the basis of the K565RUZ microcircuit;

an integration module with standard Elektronika OZU-64K memory unit;

a peripheral device control module that permits the Videoton-340 alphanumeric display and the Elektronika-302 cassette tape recorder, used to store systems and debugged programs, to be connected to the OKA-80. This same module contains a programmer for writing data in the PROM with ultraviolet erasure (the plug for installation of the PROM is located on the front panel of the module);

a DZM-180 line printer, FS-1501 papertape reader and PL-150 perforator control module.

Structurally, each of the enumerated modules is based on a card measuring 170 X 200 mm, installed in a housing designed for six cards. The peripheral device integration modules are installed in strictly allocated positions and the remaining modules can be installed in any of the four remaining positions. The Elektronika OZU-64K unit included in the complex provides the maximum possible memory capacity of 64 Kbyte for the K580IK80 microprocessor. The users which the least memory capacity satisfies can utilize static and dynamic main memory modules and the corresponding memory sections of this unit are automatically switched off during joint operations of these modules with the Elektronika OZU-64K unit. The present of various main memory units in the OKA-80 complex permits debugging of hardware of these main memories by connection of the cards to be processed to the complex. The processor module is integrated to the peripheral devices by using K580IK55 BIS [large integrated circuit]. The integration modules with the input-output devices of the Elektronika-100I minicomputer and the integration modeul with interface T, which permits connection of up to eight peripheral devices having the indicated interface to the complex, were developed to expand the nomenclature of the peripheral devices with which the OKA-80 can operate. The systems software of the OKA-80 complex includes a control monitor, which supports debugging operations, a text editor, an absolute macroassembler and program interpreters in Basic language.

The first version of the control monitor occupies a memory capacity of 1 Kbyte. This monitor is written in the PROM. The second version requires 4 Kbyte of memory and has considerably greater capabilities in program debugging. This monitor is entered in the memory of the complex from papertape and during its operation the PROM with the small monitor can be switched off by using the toggle switch on the front panel of the corresponding module. The control monitor permits (Figure 2):

input of programs and data to the memory from papertape or magnetic cassette and retrieval from the memory to papertape or cassette;

editing of the contents of the memory cells, internal registers of the processor and registers of the external ports;

Functions of MONITOR Program

Data Input-Output

II--input from papertape in 16-bit format
OI--output to papertape in 16-bit format
IT--input from papertape in absolute format
OT--output to papertape in absolute format
IL--input from tape recorder
OL--output to tape recorder
IK--input from display keyboard
D--output to display and alphanumeric printer
OM--output to display and alphanumeric printer in assembler mnemonic code
IM--input in assembler mnemonic code

Display and Editing of Contents of Memory Cells and Registers of Microprocessor

A--editing of contents of memory cell
HA--output of contents of processor registers
HM--editing of contents of processor registers
HP--editing of contents of peripheral device registers
HC--filling main memory with constant
HU--shifting of main memory

Comparison and Search

HX--comparison of two main memory regions
HV--comparison of data on papertape to contents of memory
HS--search in region of memory cells with given contents
HT--test of memory

Starting of Program

S--start of systems programs
U--start of user programs
G--start of user programs in debugging mode
B--start of BASIC interpreter

Figure 2. Directives and Functions of MONITOR Programs

shifting information to the memory and filling in sections of the memory with a constant;

comparison of the contents of different sections of memory and also the contents of a section of memory to data on papertape;

retrieval of the contents of sections of memory to a display screen or printout in the form of a table or in the mimic flow sheet of the assembler;

startup for implementation of a user program or individual sections of it with routing by jump instructions.

An interrupt circuit by instruction of the user program, by means of which control is transferred to the monitor after execution of each instruction of the user program, is employed for work in the routing mode. Command execution of the user's program can be realized by using this circuit. Besides the indicated capabilities, the capability of testing the memory of the debugging complex and of determining the boundaries of the main memory available to the user is also provided in the monitor. The text editor is used to prepare the programs in macroassembler or Basic language and represents a program that permits entry of arbitrary text from papertape or display keyboard to the memory, making changes in this text and retrieval of the corrected text to papertape. The input macroassembler language completely corresponds to the macroassembler of the Intel Company for the 8080 microprocessor. The macroassembler generates an absolute object code. The interpreter of Basic language contained in the software of the complex occupies 6 Kbyte of memory and permits development of a program for processing numbers with floating point and symbolic data. There is a simpler interpreter from this language, which occupies 2 Kbyte of memory, for programs that work only with integers. When developing the software, the user can select one or another configuration of the debugging complex, the peripheral devices required by him and systems software for a specific system based on the K580IK80 microprocessor.

Development of the program in assembler language using the OKA-80 debugging complex consists of the following main steps:

1) preparation of the input program in assembler language using the TEXT EDITOR systems program;

2) translation of the initial program to microprocessor codes by the MACROASSEMBLER program;

3) debugging of the translated program using the debugging devices of the MONITOR program.

If serious errors, correction of which by devices of the MONITOR program is difficult, are determined during debugging, one must return to the first step, make the necessary corrections in the initial text of the program to be developed and repeat steps 2 and 3.

A significant disadvantage of the OKA-80 is the absence of large-capacity external memories, which reduces the user's work efficiency somewhat. The KSI-1 cross system for development of software for the K580IK80 microprocessor is devoid of these deficiencies. This cross system (Figure 3) is a set of programs for the SM-4 universal computer and it includes a translator from assembler language to codes of the K580IK80 microprocessor, a simulator of the instruction system of the K580IK80 microprocessor and a debugging monitor.

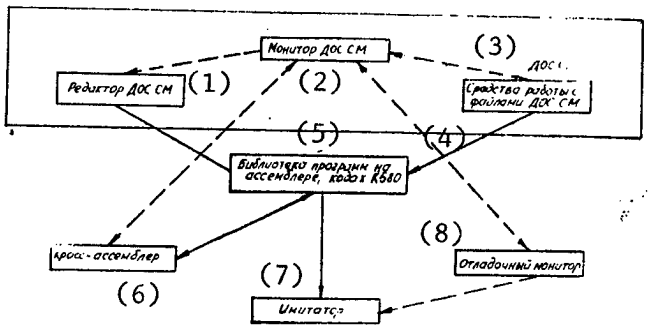

Figure 3. Structure of KSI-1 Cross System

Key:

1. Editor of SM disk operating system
2. Monitor of disk operating system
3. SM disk operating system
4. Devices for working with files of SM disk operating system
5. Library of programs in assembler and K580 codes
6. Cross assembler
7. Monitor
8. Debugging monitor

The KSI-1 cross system functions within the SM disk operating system DOS SM and is actually a subsystem of it. Standard devices of the SM disk operating system are used to enter program texts in assembler language or in the instruction system of the microprocessor and to write them in the form of files on disk, for editing of program texts, for printout of programs or output of programs to papertape and management of libraries of debugged programs.

The assembler language of the KSI-1 system does not permit the use of the MACRO pseudoinstruction and conditional assembly. It completely corresponds to the assembler language of the OKA-80 hardware-software complex in the remaining features. The translator occupies a capacity of 20 Kwords. The object codes of the program to be debugged, found as a result of translation by the cross assembler, are arranged in the least significant bytes of 2-byte words of the MEM array (Figure 4). The most significant bytes contain 7 single-bit characters:

the character for debugging output of the contents of registers or of given memory cells after execution of the given instruction DFT;

the program interrupt character after execution of the given instruction AIP;

the character of the data byte CBD;

the character of the first byte of the instruction GBC;

the character of the presence of a label FLA;

the character of a check stop after execution of given instruction CSP;

the character of memory protection to write KMW.

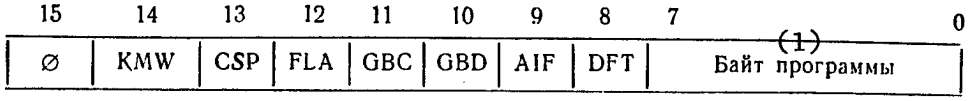

Figure 4. Element of MEM Array

Key:
1. Program byte

The most significant bit of a 16-bit word always has the value zero. The value of the index of the MEM array is the address of the memory cell. Moreover, the database of the simulator (Figure 5) includes variables that simulate the instruction counter (PC), the stack pointer (SP), the accumulator (A), 6 POH (B, C, D, E, H, L), single-bit result characters (S, Z, P, C, AC) and interrupt authorization flip-flop (T1). A clock counter T is also introduced. The time of execution of the instruction by the microprocessor in the machine clocks is added to the contents of the counter upon execution of each instruction of the program to be debugged. The contents of the clock counter are brought out to the display screen upon interrupt, check stop or after execution of the program. The database also includes a stack for storage of the status of the program, an address table of variables retrieved during routing, a label table created by the cross assembler and characters of the debugging modes.

The interpreter is a set of subroutines corresponding to groups of instructions of the microprocessor. These subroutines are combined into a single whole by the program-instruction decoder. The interpreter begins its work upon assignment of directive E (Execute) or S (Step) by the user. The independent variable of directive E is the address of the program start. This address is entered in the memory cell, which simulates the instruction counter of the microprocessor. The instruction code arranged according to the entered address is selected from the MEM array and is decoded. The remaining instruction bytes are then selected from the MEM array if necessary and they are executed. The given routing modes and the status of different characters (for example, the check stop character) are analyzed during execution of the instruction. If this is necessary, the program status is stored, the contents of the registers and cells are retrieved and so on.

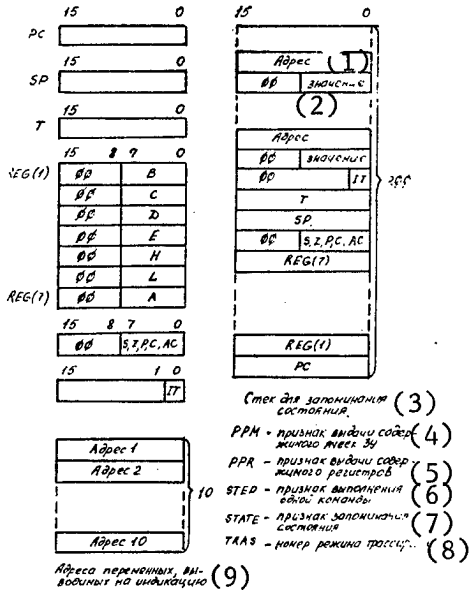

Figure 5. Database of Simulator

Key:

1. Address
2. Value
3. Stack for storage of status
4. Character for output of contents of memory cells
5. Character for output of contents of registers
6. Character for execution of one instruction
7. Character for storage of status
8. Number of routing mode
9. Addresses of variables brought to display

The overlap system of the SM disk operating system was used in writing the simulator.

The simulation subroutines of the instruction system are divided into 20 files located on a magnetic disk. The resonant part of the simulator occupies 15 Kwords of the main memory and each overlap occupies up to 5 Kwords. The total capacity of the simulator comprises approximately 115 Kwords. The debugging monitor provides interaction of the user with the cross system by interpretation of the directives entered from the display keyboard. The debugging monitor and the simulator use the same database. All the directives of the monitor are divided into control and debugging directives. There are two control directives: R (read assembled module to MEM array) and O (conversion to debugging mode). The object program found by using the translator from assembler language or by introduction into the program library in binary form is rewritten by directive R to the SM-4 memory. Directive O transfers control of the debugging directives, a list of which is presented in the table, to the interpreter.

Debugging Directives of KSI-1 System

Type of Directive	Description
E <address>	Start of program from given address. If address is not indicated, then from address in PC
S	Execution of one instruction
C	Storage of program status
V	Restoration of program status
D <address 1>, <address 2>	Retrieval of memory contents from address 1 to address 2
D <address> : <byte>	Writing of byte in memory according to given address
L	Retrieval of register contents
L <register> : <byte>	Writing of byte in indicated register
B <address 1>, ..., <address n>	Setting points of check stop
F <address 1>, <address 2> : <constant>	Retrieval of one-, two- or three-byte constant
O <address 1>, ..., <address n>	Assignment of addresses of variables retrieved during routing
T1	Assignment of first routing mode: printing of labels
T2	Assignment of second routing mode: printing of instruction codes of control transmission
T3 <address 1>, ..., <address n>	Assignment of third routing mode: print contents of registers and memory cells after execution of instructions with indicated addresses
TØ	Replacement of routing modes
W	Display of output data
P <address 1>; <address 2>	Protection of memory cells from address 1 to address 2 to write
Z <address 1>; <address 2>	Replacement of protection to write
A <PR:A	Input of program to be debugged from papertape
A >LP:	Printout of program

The cross system is compatible with the OKA-80 hardware-software complex at the level of assembler language and papertapes. By combining the advantages of the cross system such as the capability of organizing the libraries of input and debugged programs, simulation of the external working situation of the microprocessor device and the advantages of the OKA-80 in real-time program debugging, the developer of microprocessors can achieve a significant reduction of development periods.

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STRUCTURAL APPROACH TO DESIGN OF MULTIPROCESSOR DATABASE MANAGEMENT SYSTEM

Leningrad IZVESTIYA VYSSHIKH UCHEBNYKH ZAVEDENIY: PRIBOROSTROYENIYE in Russian No 9, Sep 83 pp 15-24

[Article by N. P. Vashkevich, S. A. Zinkin and V. P. Kulagin, Penza Polytechnical Institute]

[Text] The problems of using the apparatus of structured networks [5] in design of a multiprocessor database management system are considered. Development of a system that performs the division operation in a relational database is given as an illustrative example.

Methods of data processing considered as a unified whole have recently become widespread. The totality of related data stored jointly forms the database (DB). Existing database management systems (SUBD) are usually constructed in the operating environment of the general-purpose computer. Realization of the SUBD functions in a dedicated processor, which has been named a database processor, makes it possible to relieve the main computer of performing database management functions and to increase the speed of execution of operations in fulfilling the requests of users by parallel calculations.

The purpose of this paper is to develop an approach to design of a multiprocessor database management system (MVS), upon use of which the hierarchical structuring of the hardware and software of the microprocessor computer system can be taken into account.

An MVS which performs relational database (RBD) management functions is considered as an example. A number of designs of the RBD processor is now described in the literature [1, 2, 3, 4]. The characteristic feature of many designs is that their realization envisions the presence of a large-capacity associative memory or storage of uniform files in the memory (ZU) with loop access. In this case the file or file segments are stored permanently in the memory sections with separate inputs. Due to the fact that most industrially-produced large-capacity dish drives (100 MBytes or more) have only one information path per group of single-module read-write heads, an MVS in which files are stored in local memory only during execution of the given operation makes sense. The files as a whole however are stored in large-capacity disk units.

Structure of the MVS. The structure of the multiprocessor system, presented in Figure 1, contains a set of uniform processor elements (PE), connected to a common bus and common memory. The processor element (Figure 2) consists of a processor (PR), local memory (LP) and a number of units (BS) for realization of parallel-process synchronization operations and for duplication of the processor element. One of the processor elements performs network control functions of the processor element. The local memory is divided into two parts: the region of the operating system (OS) and the data region (OD). The operating system module is stored in the region of the operating system and segments of the input relations and results are stored in the data region. To provide functional independence, each processor element has available a complete set of relational algebra operations, which consists of two groups: set operations (join, intersection, subtraction and Cartesian product) and specialized relational operations (restriction, projection, union and division). The processor element, which executes control functions, realizes data input-output operations, synchronization of parallel processes and organization of replacement of malfunctioning processor elements. The common memory or working region (RO) of the MVS serves to form the final results of the performed operations.

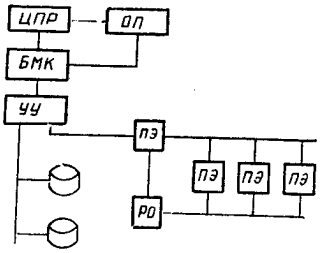

Figure 1. Block Diagram of MVS: TsPR--central processor; OP--main memory; BMK--unit multiplex channel; UU--control device; PE--processor element; RO--working region

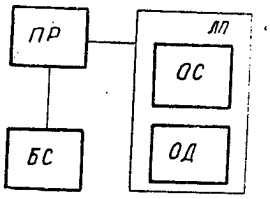

Figure 2. Structure of Processor Element: PR--processor; BS--synchronization unit; LP--local memory; OS--module of operating system; OD--memory module for storage of input data of result

The MVS user interface. There are now several approaches to construction of languages based on relational algebra (RA) and on relational calculus (RI) [5, 6]. The operator in relational algebra has one or several relations as the

operand or operands and forms a new relation according to a specific rule. The user query, written in the language of relational calculus, indicates the desired relation and allows the machine itself to decide which operations must be selected to find the needed relation from the database.

A query formed in the language of relational calculus (α-expression) is expanded by means of a reduction algorithm into a series of relational algebra operations. An expression of type

$$(t_1, \ldots, t_k) : U_1 \& U_2 \& \ldots \& U_p \& V,$$

where $t_1, \ldots, t_k$ is the sequence of line variables and cuts, U_i, i = 1, 2, ..., p is a correctly constructed formula, correctly determined on the line variable [7] and V is the quantifier part of the α-expression in which all quantifiers are advanced forward, while the non-quantifier part is transformed to normal disjunctive form, is called an arbitrary simple α-expression.

Representation of the α-expression by a sequence of relational algebra operations is the first part of transforming the user query. These actions can be realized both at the level of the MVS and at the level of the computer operating system. The second part of transformation of the α-query is optimization of access of the sequence of relational algebra operations to the database. The result of action of the optimization algorithms of the interface is transformation of the α-expression to a sequence of relational algebra operations having more effective access to the database [8, 9].

Method of Design of Multiprocessor Computer System

Working out simulation structure of multiprocessor computer system. Methods of combining the levels of modelling during investigation of complex computer systems, which have now achieved further development, were considered in [10]. The following approach to design of the structure that simulates the operation of a multiprocessor computer system is suggested with regard to the variety of functions of the MVS and their different realization by software and hardware.

Let us introduce the set $H = \{h_1, h_2, \ldots, h_n\}$, the elements of which are operations performed by the MVS. Let us set the sequence of processes (p_{i1}, p_{i2}, ..., p_{ik}) that simulates its execution into agreement to each operation. The simulation algorithm of operation h_i can then be represented by the graph of development of processes G_i. The requirement of correct embedding is imposed on graph G_i, i.e., all the components of the development graph should be described by functions of sequential coupling of processes S (a, b) and parallel coupling of processes P (a, b) [11]. The function f (S, P, p_{i1}, ..., p_{ik}) describes the simulation algorithm of operation h_i with regard to the introduced notations. Construction of the simulation algorithms of operations that meet the requirement of correct embedding is considered in [12].

Let $A_i = \{a_{i1}, \ldots, a_{im}\}$ be the block diagram of a device that realizes operation h_i, where h_{ij}, j = 1, ..., m are components of A_i. The parallellism of executing operation h_i is reflected by the number of uniform processor elements in which processes h_i occur simultaneously with different input data. Depending on the number of operations performed simultaneously, one can distinguish

two levels of parallellism: level 1--parallel execution of ℓ independent operations, each of which is realized by the subset of the processor element, and level 2--parallel execution of one operation. The overall structure of the MVS that realizes the set of operations H is determined by superposition of separate structures is:

$$A = \bigcup_{i=1}^{n} A_i$$

Structured networks, by means of which the operations of the MVS are simulated, are used in the given paper as a tool for investigation of MVS operations. The type of each network is described by structured formula F_i. The overall network that simulates operation of the MVS is found as a result of superposition of individual networks $F = (F_1, F_2, \ldots, F_n)$.

Development of MVS algorithms. Let us use Petri nets [13], which have gained wide recognition during the past few years as a convenient and descriptive formal apparatus for investigation of the qualitative characteristics of parallel systems and processes, as a device for describing MVS operations. Structured, regular and inhibitor classes of nets were introduced in [14-16]. Let us introduce the following concepts and notations to describe MVS algorithms.

The position of the Petri net displays the status of the assembly or of the device of the object to be simulated. The dynamic properties of Petri nets are used to simulate the operations of some object, where it is important to know not only the degree of occupation of the assemblies and devices by ongoing processes, but also the time distribution of the level of their use. Let us introduce the following concept of conversion of a Petri net: conversion of a Petri net shows the totality of operations of the assemblies and devices of the object to be simulated, occurring during ξ units of model time. Let us call position p "empty" if it has zero marking.

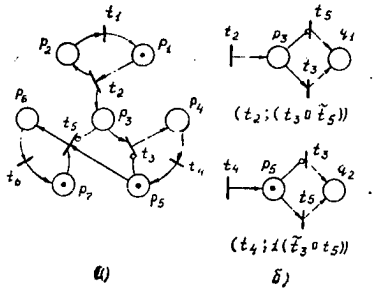

Figure 3. Fragment of Petri Net Containing Inhibitor Arcs

The class of inhibitor nets I, considered in [16], considerably expands the descriptive capabilities of Petri nets. To describe the fragments that contain inhibitor arcs, let us make use of the notations presented in Figure 3, which shows a fragment of the net (Figure 3, a) and the basic elements containing inhibitor arcs (Figure 3, b).

Design of the algorithm of division operation. Division is one of the most complex relational algebra operations, upon realization of which a number of

simpler operations must be used. Let us consider the algorithm of the division operation in the following example.

Let the following query be formulated to relations S and SP (Figure 4): find the names of those suppliers which do not deliver part P1. In terms of relational calculus, the given query appears as follows:

$$(S.NAME): \neg \exists SP(SP.S\# = S.S\# \ \& \ SP.P\# = 'P1')$$

or in normal form

$$(S.NAME): \forall SP(SP.S\# \neq S.S\# \vee SP.P\# \neq 'P1').$$

S is the initial relation in which the domain S# is the dividend (DLM) and the domain NAME is the compliment (DPL). The pair (S#, NAME) forms the procession (element) of relation S. SP is the relation-divisor (DLT). To describe the algorithm, let us introduce the dividend ODLM and divisor ODLT regions with volumes V_{ODLM} and V_{ODLT}, respectively. The volume V_{ODLM} permits distribution of p processions of relation S. Volume V_{ODLT} corresponds to one procession (element) DLT. The essence of the algorithm is that all the initial relation is considered for each DLT element. The result of division of relation S by the i-th element of relation SP is registered in the region of the division result (array RDEL--i-th column) with volume V_{RDEL}. Intersection of the subsets determined by the contents of the columns of the RDEL array yields the final result of the operation of dividing relation S by SP.

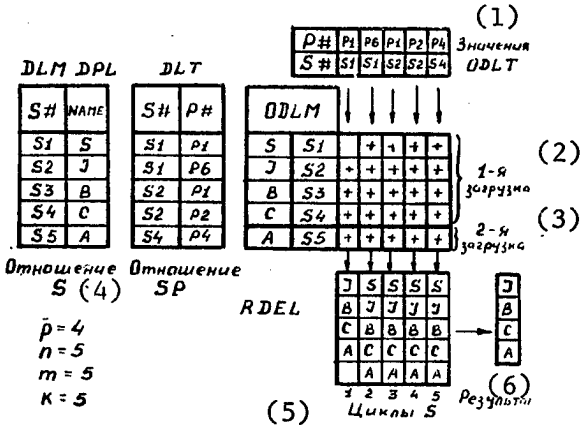

Figure 4. Diagram of Performing Division Algorithm

Key:

1. Values
2. First loading
3. Second loading
4. Relation
5. Cycles
6. Results

When realizing the considered algorithm in the MVS, the analogs of the values presented in Figure 4 will be: $V_{ODLM} + V_{ODLT} + V_{RDEL}$ is the volume of the data region of the processor element, RDEL is the total memory of the MVS, the volume of which should not be less than V_{RDEL} for effective execution of the

intersection operation; the number of cycles of elements S is the number of processor elements in the MVS. The variables n, m, p and k determine the number of elements of the initial relation, the number of divisor elements, V_{ODLM} and the number of processor elements, respectively. A Petri net, which simulates the division operation according to the outlined algorithm, is presented in Figure 5.

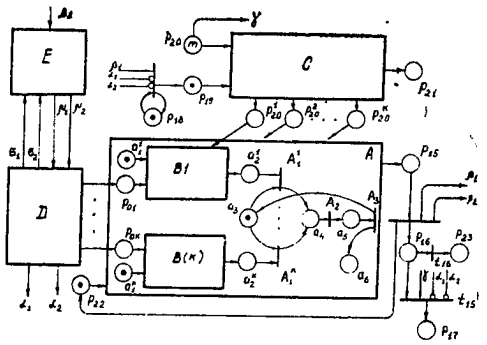

Figure 5. Structured Petri Net That Simulates Division Operation of Relational Algebra

Description of operation of the net. The following structured formula determines the net presented in Figure 5:

$$(t_{14};\ 1A;\ t_{14};\ t_3;\ 1t_1;\ t_2),\ (t_{11};\ t_6;\ t_5;\ t_4),\ (t_7;\ t_8;\ t_9;\ t_{10}),$$
$$(t_2;\ (\tilde{t}_{10}\square\tilde{t}_4\square t_3)),\ (t_4;\ (t_7\square\tilde{t}_{10}\square\tilde{t}_{13}\square\tilde{t}_{15}\square\tilde{t}_2)),$$
$$(t_{10};\ (t_{11}\square\tilde{t}_4\square\tilde{t}_{13}\square\tilde{t}_{15}\square\tilde{t}_2)),\ (t_{12};\ (t_6\square t_8)),\ ((t_7\square t_{11});\ t_{12}),$$
$$(m(C_1\square\tilde{t}_{15})),\ (1^*t_{13};\ 1C),\ (t_{14};\ (t_{15}\square t_{16})),$$
$$((C_2^1;\ B1_3),\ (C_2^2;\ B2_3),\ldots,\ (C_2^k;\ B(k)_3)),$$
$$((t_{12};\ B1_1),\ (t_{12};\ B2_1),\ldots,\ (t_{12};\ B(k)_1))$$
$$B(i):\ (\tilde{B}(i)_1;\ B(i)_2{}^1;\ B(i)_2{}^2;\ldots;B(i)_2{}^p),$$
$$(B(i)_2{}^p;\ (\tilde{B}(i)_4\square B(i)_1)),\ (B(i)_3;\ {}^*B(i)_4),$$
$$(1^*B(i)_1;\ B(i)_{11}),\ (B(i)_4;\ ((B(i)_5;\ B(i)_6;$$
$$B(i)_7;\ B(i)_8)\square(B(i)_{10};\ B(i)_9))),\ 1\leqslant i\leqslant k$$
$$C:\ (1^*C_1,\ (^*\tilde{C}_1;\ (C_2{}^1\square C_2{}^2\square\ldots\square C_2{}^k)),\ (1C_2{}^1;\ C_2{}^2;\ldots;\ C_2{}^k))$$
$$A:\ (1(B1,\ B2,\ldots,B(k)),\ (B1;\ A_1{}^1),\ (B_2;\ A_1{}^2),\ldots,$$
$$(B(k);\ A_1{}^k),\ (^*(1(A_1{}^1\square A_1{}^2\square\ldots\square A_1{}^k);\ A_2;\ A_3))),$$

where the symbols ';', '*', '□', ',', $n(\ )$ denote addition, iteration, exclusion, superposition and marking operations, respectively [14]. This formula gives the initial marking and the structure of transitions and serves for formal determination of the net under investigation. The priorities pr of transitions $A1^1\ldots$, $A1^k$ are correlated in the following manner: $prA_1{}^1 > prA_1{}^2 > prA_1{}^3 > \ldots > prA_1{}^k$. Transitions t_2, $B(i)_1$, t_{15} have equal priority and higher priority with respect to the remaining transitions.

The following sequence of operations is realized in the MVS according to the described net: each processor element receives a DLT element distinct from the others, the result of division of relation S by element DLT of the i-th processor element is determined, the operation of intersection of the partial result of the i-th processor element with the result stored in the common memory of the device is performed, the result of the intersection operation is placed in the common memory of the device, the device completes its own work when the following levels are completed: division by all DLT elements, all elements S are considered for elements DLT placed in the processor element upon subsequent loading and all processor elements have completed work.

The structured transition C (Figure 6) describes loading of the processor element by DLT elements. As a result of initial marking, position p_{20} contains m labels, the number of which determines the dimension of the divisor array. Upon activated transition C (the presence of a label in position p_{19}), the label is shifted from position p_{20} to position c_3. The inhibitor arc that links position c_3 to transition C_1 prohibits the number of labels greater than 1 being located in position c_3. The label placed in position c_2^1 during initial marking is shifted by positions c_2^2, c_2^3, ..., c_2^k during operation of transition C, opening simple transitions C_2^1, C_2^2, ..., C_2^k. This permits loading of DLT elements into the processor element according to the increase of the ordinal number. Transition C completes its work in the absence of labels at the local inputs (positions c_2^1, c_2^2, ..., c_2^k) to internal transitions C_2^1, C_2^2, ..., C_2^k. The structured transition C can be activated if the following conditions are fulfilled: the presence of a label in output position p_{15} of structured transition A (all processor elements have completed work), the absence of labels in positions p_{12} and p_5 (the processor elements have completed the last part of relation S in performing division operations by DLT elements loaded into the processor element.).

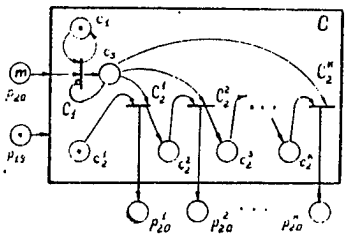

Figure 6. Structured Transition C

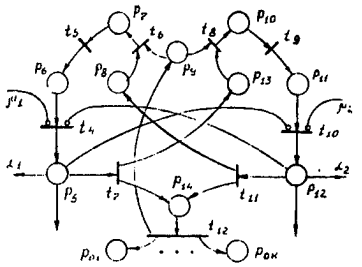

Figure 7. Fragment D

Fragment D (Figure 7) describes the circulation of elements S and their transfer to the memory of the processor element. According to the algorithm to be realized for determination of the result of division S by the element of the i-th processor element, each element of the dividend should be compared to element DLT placed in the i-th processor element. Circulation of elements S is realized in the following manner: two buffers (P_1 and P_2) with capacity of n elements are introduced, element S emerging from buffer P_1 (P_2) enters the memory of all processor elements and buffer P_2 (P_1). Freeing of one buffer activates connection of another. The number of loops of elements of relation S is determined by the number of DLT elements that have passed through one processor element. The initial marking determines the presence of n labels in position p_{11}, which corresponds to nS elements in buffer P_1. At the beginning of simulation, transition t_{10} is excited (positions p_3 and p_5 do not contain labels), which permits the label of position p_{12} to be used. The label is transferred from position p_{12} to positions p_{14} and p_8. Position p_{14} is linked to positions p_{01}, p_{02}, ..., p_{0k}, which are the external inputs of structured transitions B1, B2, ..., B(k), which simulate the operation of the processor element, and to position p_9, which is linked to positions p_6 and p_{11} through transitions t_6 and t_8. However, the presence of a label at position p_8 and the absence of it at p_{13} permits response only to transition t_6, as a result of which a label to be placed in position p_6 (the element of the initial relation was transferred from buffer P_1 to buffer P_2). Transitions t_4 and t_2 will be closed until labels are located in position p_{12} (buffer p_1 contains the elements of the initial relation).

If n > p, then further influx of labels to structured transitions B1, B2, ..., B(k) (Figure 8) through external inputs p_{01}, ..., p_{0k} must be stopped after simulation of loading the memory of the processor element. This is realized by introduction of inhibitor arcs that link positions b^p_{11}, b^p_{21}, ..., b^p_{k1} to transitions $B1_1$, $B2_1$, ..., $B(k)_1$. Until the condition is fulfilled at which position b^p_{i1} is empty and position p_{01} contains a label, transition $B(i)_1$, having higher priority with respect to transition $B(i)_{11}$, is triggered. As soon as the label is carried to position b^p_{i1}, which corresponds to acceptance of pS elements by the memory of pe_i, transition $B(i)_1$ is converted to the passive state. Transitions $B(i)_3$-$B(i)_{10}$ and positions b_{i2}-b_{i8} simulate the operation of comparing the DLT element of the i-th processor element (the presence of this element is simulated by a label in position b_{i2}) to the contents of the memory of pe_i. Position b_{i3} simulates selection of the branch of the net as a function of the result of comparing the DLM element to the DLT element. Structured transition B(i) converts to the passive state when none of its internal transitions can respond due to the absence of labels at some local inputs. Conversion of transition B(i) to the passive state is accompanied by the appearance of a label in output position a^i_2, which causes restoration of the initial marking in transition B(i), but not activation of it.

Transitions A^1_1-A^k_1, A_2, A_3 and positions A_3-A_6 (Figure 5) simulate the operation of the assemblies of the device in intersection of the result of the

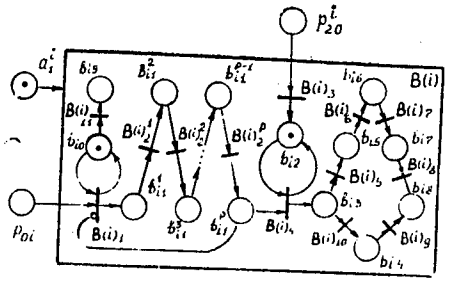

Figure 8. Structured Transition B(i), $1 \leq i \leq k$

division operation in the i-th processor element with the contents of the working region. Due to the fact that the assembly to be simulated can work with only one processor element, devices must be introduced that eliminate the appearance of blind alleys in functioning of the entire system. This is achieved by introduction of an arbiter, which is simulated by position a_3 linked to transitions (A_1^1-A_1^k) of all processor elements. Completion of operation of structured transition B(i) (the presence of a label in position A_2^i) excites the simple transition A_1^i, upon response of which the label is removed from position a_3. The absence of a label at position a_3 prohibits the response of simple transitions A_1^1- A_1^{i-1} and A_1^{i+1} - A_1^k. After the intersection is fulfilled (response of transition A_3), the label is moved to position a_3, which leads to excitation of the transitions, according to which the structured transitions have completed their work. The priority of response of the transitions in this phase is determined by the priorities assigned to them. One of the problems to be solved in simulation of the operation of the device is to determine the number of assemblies that accomplish the operation of intersection of the partial results of the processor element within minimum time. Assigning the number of these assemblies in a network is reflected by placing the corresponding number of labels in position a_3. The completion of work of structured transition A is the status of completion of structured transitions B1-B(k) and the passiveness of simple transitions A_1^1-A_1^k, A_2 and A_3 due to the absence of labels at the local inputs. Conversion of transition A to the passive state is accompanied by placing a label in position p_{15}, after which the initial marking of the internal points of the subnet of transition A and activation of it (carrying the label to position p_{22}) are restored. Restoration of the initial marking of subnet A activates the nets of structured transitions B1-B(k), as a result of which simulation of a new load of the processor element and execution of the divion operation begin.

If buffer P_1 (or P_2) contains n' elements and n' < p before the next loading of the processor element, the entry of elements from buffer P_2 (or P_1) to the memory of the processor element must be closed in this case to maintain the veracity of the result of the division operation and simulation of the division operation must be begun with incomplete loading of the memory of the processor element. Fragment E (Figure 9) is included in the net for this purpose. At the beginning of simulation, which is characterized by the absence of labels at positions p_{12} and p_5, transition t_2 cannot respond due to the absence of a label at position p_2. Conversion of the label from position p_1 to position p_2 coincides with prohibition of operation of

transition t_2 by the presence of a label at position p_{12} (or p_5). As a result of this organization of couplings, position p_3 remains empty and does not forbid operations of transitions t_{10} and t_4. Transition t_2 is excited only if positions p_{11} and p_{12} or p_6 and p_5 are empty. This status of subnet D causes excitation of transition t_4 (or t_{10}). However, transition t_2 responds due to the higher priority with respect to transitions t_4 and t_{10}, as a result of which the work of transitions t_4 and t_{10} is forbidden and access of labels to position p_{14} is stopped. The passive state of transition $B(i)_1$ authorizes transition $B(i)_1$ having lower priority to respond. The external input of structured transition B(i) is switched off by this until transition B(i) completes simulation of the division operation in pe_i and restoration of the initial marking in internal net B(i).

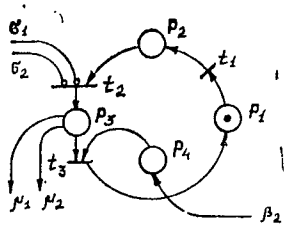

Figure 9. Fragment E

Subnet D will be in the passive state until completion of the work of structured transition A. Placing a label in position p_{15} (Figure 5) and triggering of transition t_{14} cause removal of the label from position p_3 and excitation of transition t_4 (or t_{10}), activation of transition A, excitation of transition t_{13}, which leads to switching the subnet of structured transition C on, and placing a label in position p_{16}. The presence of a label in position p_{16} excites transition t_{16} and contributes to excitation of transition t_{15}. A higher priority is assigned to transition t_{15}; therefore, transition t_{16} can respond only if transition t_{15} is in the passive state. Position p_{23} can serve as a counter of the number of cycles of elements of relation S.

The work of the structured net that simulates execution of the division operation will be continued until the following conditions are fulfilled: position p_{20} is empty (the last divisor elements are loaded into the processor element), positions p_{12} and p_5 are empty (elements S completed the next transition from buffer $P_1^{12}(P_2)$ to buffer P_2 (P_1)), completion of transition A (the work of the processor element is completed and the operation of intersection of the results of fulfilling the division operation with the contents of the working region was performed). The response of transition t_{15} and placing a label in position p_{17} leads to completion of functioning of the structured net.

The considered net describes the operation of the units of the block diagram of the MVS (Figures 1 and 2) according to the scheme of executing the division algorithm (Figure 4). One can conclude from analysis of the structure and model that the functions of an operating processor element are determined by structured transition B (i). The remaining fragments and structured transitions of the net determine the operation of the control processor element.

It is shown in the given paper that an approach based on the use of structured Petri nets permits development of the hardware and software of multiprocessor database management systems with regard to the hierarchy and relationship of the levels of representation of the system. Formalization of the structure to be analyzed permits easy alteration of the achitecture of the MVS and organization of the automated design of computer systems. The approach outlined in the given article can be used in development of other complex computer systems and complexes.

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CSO: 1863/13

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IMAGE INPUT/OUTPUT CONTROLLER-INTERFACE BASED ON 16-BIT MICROPROCESSOR

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 83
(manuscript received 6 Oct 82) pp 7-12

[Article by A. M. Ostapenko and V. A. Sluyev (Novosibirsk)]

[Text] Image processing problems are solved with systems including a large complex of hardware and software. Computers are used to implement many functions in controlling image I/O devices, processing images and outputting results as generalized characteristics or images on photo material or a display screen. The class of computers now used for processing data recorded on a photograph is quite specific and the more complex the processing algorithm and greater the volume of source information obtainable in digitizing the photograph are, the higher the throughput and memory size, etc. required. Ignoring the data processing question, let us consider the problem of obtaining data, i.e. the systems aspect of operating with the computer I/O device. It involves problems of device control, buffering and transfer of data in the format required by the processing computer, providing necessary and where possible advanced facilities for interaction with respect to the specifics of the entire system as a whole.

In this article, we describe a system which includes an Optronics image I/O unit and the SM-4 minicomputer connected by using a controller-interface based on the TMS 9900 16-bit microprocessor.

The Optronics family of scanners which includes the P-1500, C-4500, L-5500 laser recorder, etc. uses a rotating drum; a photograph is placed on the drum for scanning by one coordinate; it also uses an illuminator and detector movable discretely for the other coordinate [1]. A domestic device of this type is described in [2]. As a rule, all these devices function within minicomputing complexes. Interfaces for computers such as the PDP-11, the Alpha-16 [1] and Computer Automation equipment have been developed and are in use. All existing interfaces are based on fixed logic and use programmable I/O for controlling the scanner and DMA [direct memory access] channel for data transfer. In operating with this interface, the computer fully controls the image scanning process by executing a set of routine operations at the level of device commands. Thus, the operation for moving the scanner carriage to a certain position requires executing several dozen instructions in a program. This leads to general reduction in computer system throughput and

unwarranted waiting for device readiness in scanning, which is especially undesirable when there are large volumes of information. To raise scanner speed and make computer capabilities more efficient, the control function has to be transferred to a separate minicomputer.

The state of modern elements, and use of LSI microprocessors and semiconductor memory allow not only developing an intelligent interface capable of efficiently operating in line with the computer with time sharing, but also placing on it some types of image processing which are conveniently performed locally at the interface level. The functions executed by this controller-interface are largely governed by a rather easily modifiable program in the base microprocessor and a minimal set of equipment added to a microcomputer.

Implemented in this controller are: efficient data buffering, scanner control operations, some types of image processing, generation of test images and various characters and the capability of simultaneous control of two devices.

Key:

1. SM-4 common bus
2. 16K x 16 memory
3. scanner #1
4. DMA
5. register
6. 9900 system
7. scanner #2

Shown in fig. 1 is a general diagram of the controller system. Broken lines indicate optional devices which can be connected by special plugs. A more detailed diagram is shown in fig. 2. Function of the individual units is described below.

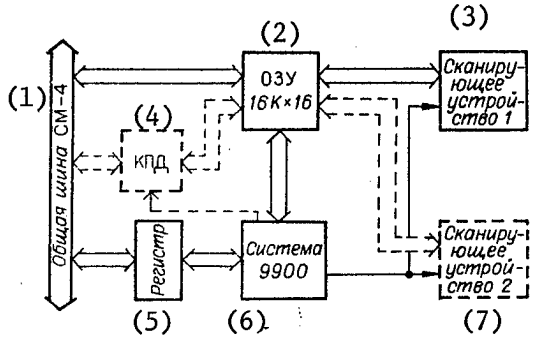

Fig. 1.

The multiport memory is the system nucleus through which data is exchanged between the computer, scanners and microprocessor. Scanner data input presupposes recording the information on mass storage, magnetic disks or tapes, since main memory size as a rule is too small to store even a small fragment of a photograph. Shown in fig. 3 is the number of data moves executed by the computer in the different versions of controller organization: program I/O, direct access channel and dual-port memory. In the latter case, controller memory is used as an extension of computer memory. The second port is fully serviced by the controller and does not require computer attention. Controller multiport memory, as an extension of computer memory, is allocated to the data buffer during scanner operation, while in other cases it can be used in any way.

The multiport memory has five ports; two are used for connecting optional devices. As a function of the port serviced, the memory is organized as 16K x 16 or 32K x 8 bits. Service is on a priority basis. Let us list the channels

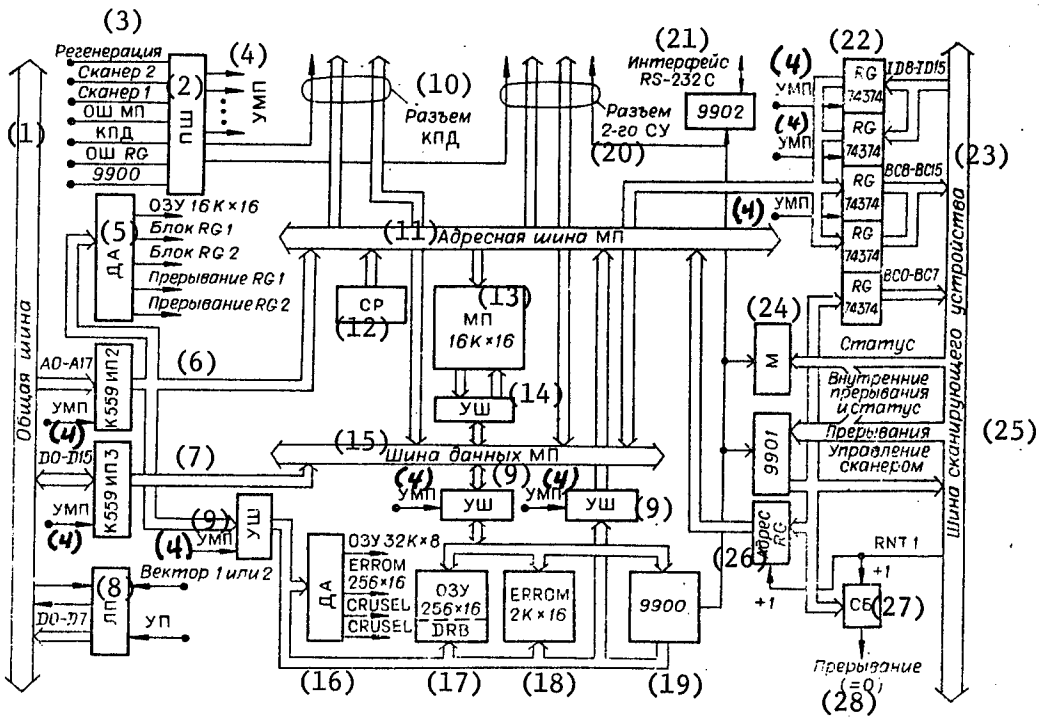

Fig. 2. Detailed diagram of controller.

Key:

1. common bus
2. PSh (priority coder)
3. regeneration
   scanner #2
   scanner #1
   OSh MP [multiport memory common bus]
   KPD (direct access channel)
   OSh RG [RG common bus]
   9900
4. UMP (multiport memory control)
5. DA (address decoder)
   16K x 16 memory
   RG1 unit
   RG2 unit
   RG1 interrupt
   RG2 interrupt
6. A0-A17, K559IP2
7. D0-D15, K559IP3
8. LP (interrupt logic)
   D0-D7
   vector 1 or 2
   UP (interrupt unit)
9. USh (bus control)
10. KPD (direct access channel) connection
11. MP (multiport memory) address bus
12. SR (regeneration counter)
13. 16K x 16 MP (multiport memory)
14. USh (bus control)
15. MP (multiport memory) data bus
16. DA (address decoder)
    32K x 8 memory
    256 x 16 ERROM
    CRUSEL
    CRUSEL
17. 256 x 16 memory, DRB
18. 2K x 16 ERROM
19. TMS 9900 microprocessor
20. SU (scanner) #2 connection
21. RS-232C interface
22. 5 x RG 74374
    ID8-ID15
    BC8-BC15
    BC0-BC7
23. scanner bus
24. M (multiplexer)
25. status
    internal interrupts and status
    interrupts
    scanner control
26. RG address
27. SB (byte counter)
28. interrupt (= 0)

Key:

a. interface
b. CPU
c. memory
d. disk or tape
e. program I/O
f. direct access channel
g. dual-port memory

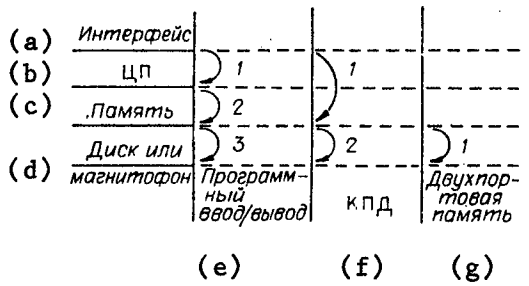

Fig. 3. Data moves executed by computer in different versions of controller organization.

connected to the ports in order of decreasing service priority: 1) channel for additional scanner connected through plug and interface board (a fast L-5500 type unit can be connected); 2) channel for the Colormation type unit; 3) channel for the SM-4 common bus; 4) direct access channel (user defines method of use); 5) microprocessor channel (the microprocessor can address 32K 16-bit words).

The memory is made with K565RU3 microcircuits and has a 1 microsecond access cycle (including time for decoding priority).

Microprocessor Subsystem. In addition to the microprocessor, the processor subsystem (see fig. 2) includes: microprocessor register storage with 256 x 16 organization; storage for programs (2K x 16) implemented with TMS2708 microcircuits; the TMS9901 parallel interface microcircuit used to control controller equipment; status bit multiplexer connected to the microprocessor in accordance with the standard for microprocessor external devices; and the TMS9902 serial interface microcircuit which allows connecting any standard RS232C device to the microprocessor.

Communication with the SM-4 central processor (TsP) [CPU] is effected through the common block of registers physically located in the microprocessor register storage. On the SM-4 side, the block of registers (BR) is located in an I/O page (higher 4K of processor address field). When the CPU accesses any register in the block, the microprocessor receives the request to use its bus by another device (request for direct access HOLD). The microprocessor completes the current storage cycle, confirms receipt of the request (HOLDA) and switches the storage control buses to the high-ohm state. On the HOLDA signal, a request for use of the multiport memory (MPP) buses is sent. In satisfying the request, a channel is formed between the MPP buses and the microprocessor through which data can be read/written from/to microprocessor register storage. Thus, the CPU has direct access to the microprocessor internal registers. This communication which makes use of TMS9900 architectural features is an extremely convenient facility for information exchange between two processors.

The L-5500 type device is connected to the controller through the scanner interface. The interface is built in accordance with the Optronics standard

for this device; therefore, any scanner meeting this standard can be connected. The data transfer channel is actually a channel for direct access to multiport memory. Control is exercised by the microprocessor through the CRU [communications-register unit] interface.

In writing (reading) data to/from film, microprocessor loads the address for the beginning of a data line to the data address register, and then the number of bytes transferred to the byte counter. After execution of a write (read) instruction, data transfer between the multiport memory and the scanner begins. Transfer of each byte is attended by incrementing of the address register and byte counter upon signal RNT1. When the byte counter reaches zero, the signal to interrupt the microprocessor is generated. The microprocessor responds to the interrupt signal at the end of a line by executing the instruction to move the carriage one step and returns to execution of the interrupted program. After completion of the carriage movement, a carriage stop interrupt signal is generated; if the image write (read) has not ended, the microprocessor repeats the operations described above until the line counter in the microprocessor register storage reaches zero.

Controller-Interface Control Unit. The central element in the controller is the TMS9900 single-chip 16-bit microprocessor [3]. It is connected to controller control units through a special I/O channel (communications-register unit) to which the TMS9901 parallel interface microcircuit and status bit multiplexer are connected. The TMS9901 microcircuit is used to output control signals (setting and clearing various flipflops, etc.) and for input of microprocessor interrupt signals.

The low-order 8 bits of the I/O bus in the TMS9901 microcircuit form a data bus byte which can be loaded into various controller registers. Bits R8-R11 define the code of the function being executed according to the pulse generated by bit R12. The function is accompanied by data on the R0-R7 bus (load of external registers) or not accompanied by them (fliflop reset and set).

Controller Programming. The central processor and microprocessor can exchange information through the register block. All registers are loaded by software by the microprocessor or the central processor and the functions of each bit are defined only by system software. Loading any code into the zero register in the register block by the central processor causes an interrupt of the program in the microprocessor to accept control information. In turn, the microprocessor has the capability of getting the attention of the central processor by setting an interrupt on the common bus (OSh). As a function of the status of the connections on the board and the coding of the common bus address decoder (DA), implemented with K556RT4 microcircuits, the register block can consist of from 0 to 32 registers for each of two scanners. The location of the block in microprocessor register storage and freedom in selecting the number of registers in the block and the functional designation of each bit allow easy modification of software during system development and operation. The current system uses 4 registers; their function is shown in fig. 4. Described below is an example of intercommunication between the central processor and the microprocessor in writing an image to film; the example clearly illsutrates the method of using the register block.

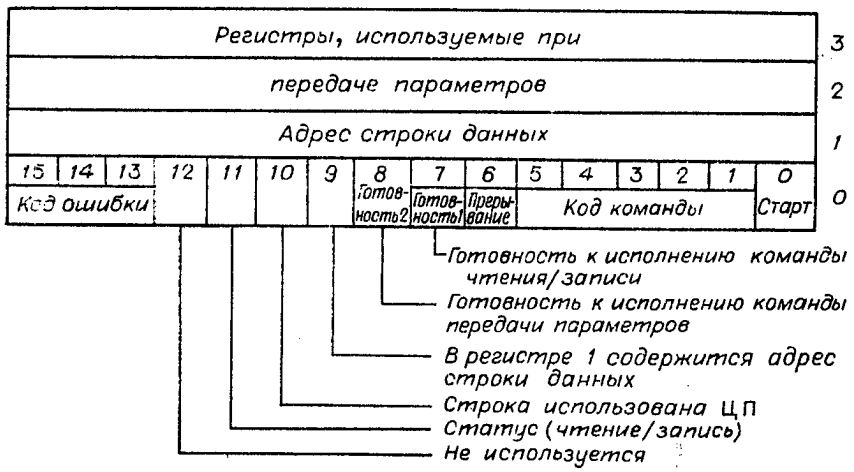

Fig. 4. Function of four registers used in system.

Key:

3, 2 registers used in transfer of parameters

1 address of line of data

0 bit:

0	start
1-5	instruction code
6	interrupt
7	ready1, ready to execute read/write instruction
8	ready2, ready to execute parameter transfer instruction
9	indicates data line address is in register 1
10	line used by CPU
11	status (read/write)
12	not used
13-15	error code

When power is turned on, the microprocessor executes a program for microdiagnostics and initial setting of internal variables and bits in register 0 in the register block. The central processor checks the status of bits READY1 and READY2 in the instruction and status register and in the case of MP readiness to accept an instruction begins executing the instruction to load parameters. Each instruction concerned with an image read/write is preceded by a series of instructions for setting parameters (frame size, transfer characteristics, etc.). The central processor loads registers 2 and 3 with the parameters and puts the instruction code into register 0 (START bit has to be set to 1). Writing the code to the zero register causes an interrupt in the microprocessor program. The microprocessor clears bit READY2, transfers the contents of registers 2 and 3 to parameter storage, sets bit READY2 and, when an interrupt is authorized by the INT bit, outputs an interrupt vector to the common bus. The address for loading parameters into microprocessor storage is governed by the microprocessor internal register which is set by a special instruction. When all required parameters have been transferred, the central processor loads an image write instruction. The microprocessor receives the

instruction, clears the bit READY1 and allocates space in data storage for the lines to be input. Then the microprocessor sends the address of the first line to register 1 in the register block, sets bit 9 in the instruction and status register and sends an interrupt to the central processor. The central processor loads the data by using the contents of register 1 as the starting address and sets bit 10 in the instruction and status register. The microprocessor requests input of new lines until the entire data buffer allocated to this scanner is full. Input line addresses are sent by the microprocessor to the ring buffer, serviced by the line processing program (POS), which is the nucleus of the controller software and is initiated when power is turned on. After processing the current line, the line processing program initiates output of the line to the scanner or when the latter is busy writes the address of the processed line to the ring output buffer. In this case, the program for output to film is initiated by a scanner interrupt (end of carriage movement by one step). Since parallel operation of two scanners is possible, the line processing program operates in the time-sharing mode. The timer for quantizing time is in the TMS9901 microcircuit. When a line will be written to film, the program handling the line end interrupt requests a new line for the free space in data storage, i.e. the microprocessor always tries to keep the data buffer full (empty when reading). When all lines are output to film, the microprocessor sets the bit READY1 and outputs an interrupt signal at which instruction execution ends. Listed below are the basic controller instructions which will be expanded as the system is operated.

1. Move carriage to origin of coordinates.
2. Move carriage relative to current position.
3. Bring carriage to specified position.
4. Move carriage to extreme right position.
5. Load address counter used in transfer of instruction parameters.
6. Write contents of registers 2 and 3 (see fig. 4) by using the address counter as the write address pointer.
7. Read according to address counter into registers 2 and 3.
8. Read address counter.
9. Read image.
10. Write image.
11. Write from character buffer, i.e. output characters.
12. Write test image.
13. Execute program from address indicated in register 2.
14. Clear instruction previously loaded.

Image Preprocessing. As indicated above, the microprocessor may be charged with some types of image processing. The complexity of the possible processing algorithms is limited by microprocessor speed, main memory size and the fact that the interface is primarily an I/O unit, not an image processor.

Taking these limits into account, we defined the following types of processing which do not substantially affect I/O speed: 1) image inversion (production of a negative); 2) nonlinear conversions; 3) image density histogram construction; 4) determination of mean illumination of the image

$$Y = \sum_{1}^{N} \frac{Y_i}{N},$$

where Y is the value of mean illumination, Y_i is i-th point density, and n is the number of points in the frame.

A prototype of the device has now been optimized and the final version based on one large multilayer board installable in the SM-4 computer I/O expansion unit is being manufactured. The system is operated under control of a software package similar to that described in [4].

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UDC 531.715.2 : 535.317.2 : 631.325.5

INDUSTRIAL OPTODIGITAL INSPECTION SYSTEM

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 83 (manuscript received 29 Mar 83) pp 53-59

[Article by V. V. Vertoprakhov, S. V. Mikhlyayev, Yu. V. Chuguy and V. P. Yunoshev (Novosibirsk) in the section "Optoelectronic Devices for Information Input, Processing and Display"]

[Text] Introduction. Developing highly productive, non-contact, precision facilities for checking geometric parameters of products is an urgent task in modern instrument making. Optoelectronic devices are considered the most promising [1]. In speed, precision and measuring range, the parameters achieved for these systems most fully meet inspection requirements

The known automatic optoelectronic systems, as a rule, allow checking products with a relatively simple shape (cylinders, tapered rollers, etc.) in one or more sections [1-4]. But modern industry needs monitors for checking products with more complex shapes; this requires information on product geometry measured in tenths or even hundredths of its sections.

There are two possible approaches to solving this problem. The first is to develop narrowly specialized devices oriented to specific types of products. This approach is warranted in the case of mass production. But when a large nomenclature of products has to be manufactured in series, it is better to develop reconfigurable (quasi general-purpose) devices that allow rapid readjustment at the hardware or software level when the product type to be checked is changed. In this case, the measuring system has to support compilation of rather complete information on product configuration; this can be done, for example, by using digital television systems based on video processors which are now in intensive development [5]. These systems allow real-time recording and storing of information on checked and reference objects and making simple comparisons. The field of application of these systems because of their low resolution ($N \times N = 512 \times 512$) is limited to basic checking of product quality and measuring geometry of small objects (1-2 micrometers) for which an error of $\delta = 1/N = 0.2$ percent is tolerable.

Measuring product parameters in a considerably larger range, down to several tenths of a millimeter, is of practical interest. In this case, traditional scanning methods can provide the required measurement precision (an error of

several micrometers, or about 0.01 percent) only when precision reading systems with high resolution (10^4 x 10^4 or higher) are used.

In checking products with a simple shape, this accuracy is also achieved in systems with conventional resolution (about 500 x 500), but with organization of the differential method of measurements [6].

Suggested in this work is a differential method for checking objects with a complex shape with distinct shadow projection which is based on Fourier optics of television and digital technology. Fourier optical methods are used to transform the contour of the shadow image of the product being checked; as a result, the spaces between its component elements are reduced tenfold. Transformed (differential) image geometry is analyzed by electronics. When product type is changed, measuring system reconfiguration can be reduced in this case to replacing the optical spatial frequency filter and the software.

Presented below is the principle for generating differential images by using the so-called dimension transforms; it was used as the base for developing the structure of an optodigital system for industrial checking; results of preliminary system tests are discussed.

Essence of Dimension Transforms. As shown in [7], generating a differential image can amount to producing multiples of the source shadow image by a certain law. This operation is efficiently implemented by Fourier optic facilities by using spatial frequency filters. Let us consider the features of these transforms using the example of two-dimensional (radial-symmetric) and one-dimensional splitting filters [8, 9].

The effect of the first filter with the transfer function

$$H(\omega) = \omega \sin(\omega D_0/2), \qquad (1)$$

where $\omega = \sqrt{\omega_x^2 + \omega_y^2}$ is the spatial frequency and D_0 is the splitting constant, when placed in the frequency range of the optical spatial filtration system [10], amounts to splitting contour 1 of the input shadow image f(x, y) (fig. 1a) into two components: the internal 2 and external 3, which are at the identical distance $D_0/2$ from the source (fig. 1b). One can see that the internal component of the output image g(x, y) is the contour of the image obtained as a result of "subtracting" area 4 from the image f(x, y) (see fig. 1b), as a consequence of which its characteristic dimension D_Δ compared to the source D is reduced by the value of D_0, i.e. $D_\Delta = D - D_0$. The transform of the image f(x, y), performed in the process, can be called dimensional, while image $g_\Delta(x,y)$, represented by internal contour 2, is differential. Let us illustrate the features of dimensional transform with the example of various objects.

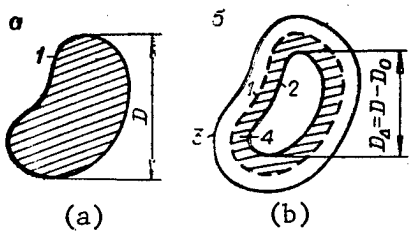

Fig. 1.

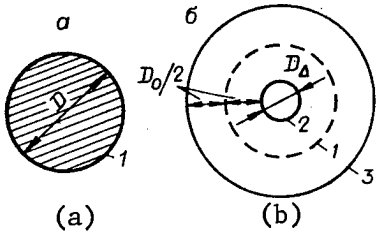

Fig. 2.

For a typical object such as a sphere (fig. 2a), the differential image $g_\Delta(x,y)$ takes the form of a circle with diameter $D_\Delta = D - D_0$, where D is the sphere diameter (fig. 2b). Let us note that in choosing $D_0 = D$, the image amounts to a point of diffraction size; this means that when the inspected size deviates from the rated by the value of ΔD, this point is transformed into a circle with the same radius of ΔD.

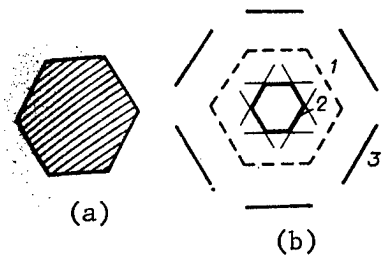

Fig. 3.

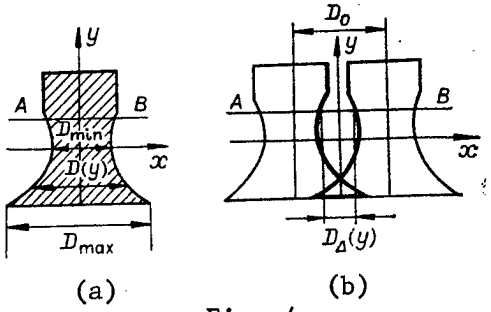

Fig. 4.

Another example is a polygon. Shown in fig. 3 is its shadow image (a) and result of filtration (b). Each segment of contour 1 in this case is split into two components 2 and 3, but because of edge effects occurring as a consequence of contour unevenness, the external components are open, while the internal are intersecting [8, 9].

Let us now take the case of a one-dimensional splitting filter described by the transfer function

$$H(\omega_x) = \omega_x \sin(\omega_x D_0/2). \qquad (2)$$

From the source image (fig. 4a), this filter forms two mapped images offset relative to each other on the x axis by D_0 (fig. 4b). The dimension of the differential image at section AB in this case is $D_\Delta(y) = D(y) - D_0$.

For the characteristic of the dimensional transform, one can introduce the coefficient of dimensional compression $\gamma = D/D_\Delta$, which defines the gain in precision when the differential method of measuring is used. The relative error of measurement in this case is $\delta = (\gamma N)^{-1}$, where N is the number of

television system resolution elements falling within the measured dimension D_Δ; when N = 500 and γ = 20, its value can be reduced to 0.01 percent. Since in the general case (see fig. 4), D(y) varies within some range $[D_{min}, D_{max}]$, it is evident the coefficient of dimensional compression $\gamma = D(y)/D(y) - D_0)$ differs for various sections of the object and is a function of D_0. In choosing the splitting constant of $D_0 = (D_{max} + D_{min})/2$, the range of variation of differential dimension $D_\Delta(y)$ is minimal: $|D_\Delta(y)| \leq (D_{max} - D_{min})/2$, therefore the coefficient $\gamma \geq \gamma_0 = 2D_{max}/(D_{max} - D_{min})$. In the worst case, when $D_{max} >> D_{min}$, the parameter $\gamma_0 = 2$. An increase in the boundary value of γ_0 is achieved when a filter in the form of superposition of components (2) with various values of splitting constants D_0 is used [7].

We used this principle for generating differential images by using dimensional transforms as the basis for developing an optodigital inspection system.

Optodigital Inspection System (OTsSK) Structure. The system includes units for optical (BOOI) and electronic (BEOI) processing of information, television (TV) camera*, microcomputer and video inspection unit (VKU) (fig. 5).

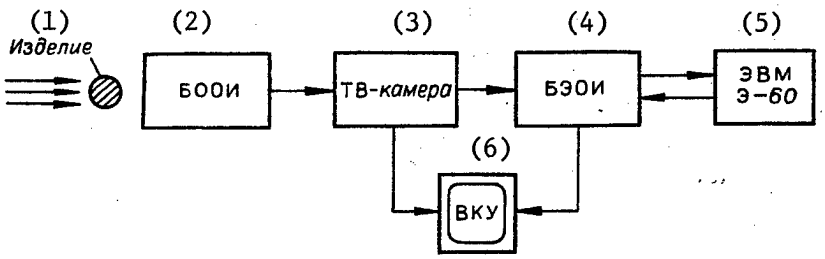

Fig. 5. Optodigital Inspection System

Key:
1. product
2. optical information processing unit
3. television (TV) camera
4. electronic information processing unit
5. Elektronika-60 microcomputer
6. video inspection unit

*
More detailed information on these units is given in the articles [7, 11] published in this issue.

The optical information processing unit performs dimensional transforms on the product shadow image. In the general case, the transform type is governed by product type and specifics of the inspection and measuring problem to be solved. In switching from one class of inspected objects to another, readjusting the optical unit in the system amounts to replacing the filter. The differential image produced at the output from this unit with the appropriate magnification is projected to the TV camera input; the video signal from the camera is then processed in the electronic information processing unit made in a standard CAMAC. Upon computer command, the electronic information processing unit converts the video signal corresponding to a specific TV line into binary form. Then the time intervals for the beginning of the TV line and the binary signal leading and trailing edges pertinent to each of the contours of the differential image at some section of it are quantized and measured. The values obtained are used in the computer to compute the x spatial coordinate at the center of each contour (the y coordinate in this case is specified by the TV line number).

Since program execution time for computing contour coordinates in a TV line is several hundreds of microseconds, this means the system can process only every third line when a standard crate controller is used. To raise system throughput, we used a crate controller with internal processing of requests [12] that allows implementing all data transfer operations within the CAMAC crate, bypassing the computer, and at a rate of several microseconds per contour coordinate. In this case, several measurements are made during a line scan (64 microseconds); thus, this system is capable of reading the coordinates of all points of the differential (contour) image in a TV frame (40 ms).

The video inspection unit displays information received from the TV camera and various service signals; this allows visual monitoring of the optodigital inspection system operation.

The system has two modes of operation: calibration and measurement.

In the calibration mode, basic system parameters are defined: splitting constants and scale (micrometers/quantum). Parameters of the standard product used in inspection by the comparison method are also input into the optodigital inspection system in this mode. This can be done at the optical level (by reading the differential image of the standard product) or by software. In the latter case, characteristic points and tolerances are specified as tables of constants.

In the measurement mode, the system records the differential image of the product being inspected, analyzes it, determines required geometric parameters and makes the decision on product acceptability. Object geometric parameters are computed by using a set of software modules executing these operations:
1. Measurement of linear dimensions (one-time measurements and those with averaging over space and time).
2. Measurement of parameters of external threads (mean diameter, step and profile angle).

It should be noted that the capability of adding to the library of software modules lends elements of universality to the optodigital inspection system.

Results from Preliminary Tests of the Optodigital Inspection System. The main aim of the tests was to define the metrologic characteristics of the system developed and to determine the requirements for precision of positioning of the product being inspected and precision of spatial filter alignment.

The optical unit in the optodigital inspection system was based on a spatial filtration system with one lens from the BP [not further identified] projector (focal distance of 200 mm, aperture of 55 mm) [7]. The spatial frequency filter aperture was 5 x 5 mm and consisted of a binary mapping component and removable one-dimensional diffraction gratings with various periods (splitting component). A He-Ne laser was used as the radiation source. Images were recorded by a KTP-87 TV camera. We used the "Elektronika-60" microcomputer. It should be noted that about 80 percent of the CAMAC modules making up the electronic information processing unit were standard.

The system optical information processing unit in tests enabled generating a differential image with 3X magnification. As a result, the scale (quantum) of the optodigital inspection system in measurements along the x and y axes was 4 and 10 micrometers, respectively. In the process, instability of measurements with respect to both electronic and optical noise did not exceed ± 2 and ± 1 quanta, respectively.

Accuracy capabilities of the system without the splitting filter (mode of projection with magnification) are illustrated in fig. 6; it shows the results of measuring coordinates of contour of a circular opening with a diameter of 0.27 mm. It follows from the drawing that the error in reproduction of the shape (half of the circle is shown) is within the limits indicated above.

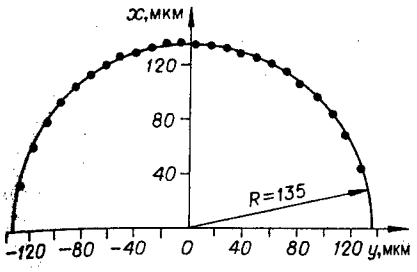

Fig. 6.

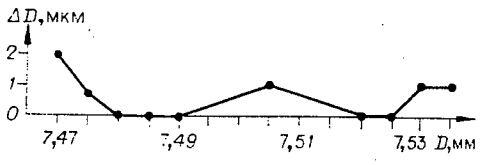

Fig. 7.

Shown in fig. 7 are results of measurement of diameters of 10 test cylindrical products. To reduce the effect of product irregularities, measurements were averaged over 30 sections of the image (on base of 0.3 mm). It can be seen from the drawing that measurement error Δ D under averaging conditions does not exceed 2 micrometers.

Shown in the following figures are experiment results illustrating the relation between measurement error ΔD and inaccuracy in positioning of the product and the splitting filter.

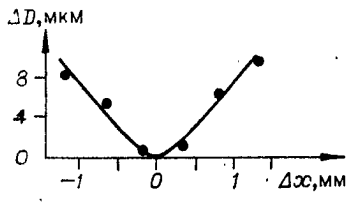

Fig. 8.

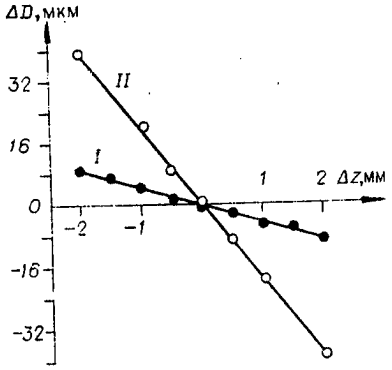

Fig. 9.

Fig. 8 shows the relation between measurement error and shifting of the product being inspected on the x axis. It can be seen that when it is shifted within the working field limits (7.5mm in the plane of the TV camera or 2.5 mm at system input), ΔD does not exceed 10 micrometers. This error is due to aberration of the optics and nonlinearity of scanning by the TV camera and can be taken into account by software.

The graph in fig. 9 (line I) shows the relation between measurement error and how much the cylindrical product image is out of focus (shifting of it (Δz) along system optical axis). It can be seen that the optodigital inspection system imposes rather low requirements on precision of product positioning: shifting of it by 0.5 mm causes a measurement error of no more than 2 micrometers. Also shown here is the relation between measurement error ΔD and filter shifting along the system axis (line II). To a large extent, its behavior depends on the parameter Δz (filter shifting by 0.25 mm produces an increase in error of 5 micrometers).

As for the relation between the error ΔD and filter shifting perpendicular to the optical axis, experiments showed that shifting of it by ± 0.1 mm has essentially no effect on the measurement result. Results obtained indicate requirements imposed on the inspected object and filter positioning accuracy in the optodigital inspection system are lower than those in the known coherent optical inspection systems [2, 4, 13].

Conclusion. Inspection of geometric parameters of products with a complex shape by direct (scanning) methods requires development of precision high-resolution measuring systems ($10^4 \times 10^4$ or more). An alternative is the differential method of measurements. To this end, using the facilities of Fourier optics and digital TV technology with conventional resolution (500 x 500) is promising. In this case, the shadow image of the object undergoes dimensional transform and is then processed by electronic facilities.

A quasi general-purpose (reconfigurable) optodigital inspection system was developed. Its optical unit was based on a spatial filtration system; the electronic unit was based on CAMAC modules and the "Elektronika-60" microcomputer. Using the CAMAC standard was rather efficient: The greater share of electronic equipment (about 80 percent) was implemented with standard modules. System quasi universality is achieved by replacing the optical spatial frequency filter and software when the product to be inspected is changed.

This system allows inspecting a broad class of products that have a distinct shadow projection, in the range to 40 mm with an error of 2-10 micrometers. In the process, information on product dimensions at 500 sections is entered into the system during a TV frame (40 ms). Processing time to define required geometric parameters is governed by the problem being solved and characteristics of hardware used in the process.

The authors are grateful to I. S. Soldatenkov for making the spatial frequency filters and to B. Ye. Krivenkov for his useful comments after he read the manuscript.

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8545
CSO: 1863/7

EFFECT OF AUTOMATED CONTROL SYSTEMS

Moscow EKONOMICHESKAYA GAZETA in Russian No 34, Aug 83 p 8

[Article by Yu. Sosin, group leader, Siberian Branch of the Central Institute of Economics and Information, USSR Ministry of Non-Ferrous Metallurgy, Krasnoyarsk]

[Text] The development of production forces in the Krasnoyarskiy Kray has led to a considerable increase in the information necessary for the efficient management of this large economic region. Economic development and structural shifts in the branches of production have rendered management of the economy substantially more complex. The main avenue toward simplification and improvement of management under these conditions is the effective use of modern computer technology.

Our kray has the necessary computer technology. At the 54 computer centers functioning on its territory there are about 180 computers, including 40 Unified System computers. By the most modest estimates, the government has spent almost 46 million rubles to build and equip them. The kray has built and put in operation 48 computerized data processing systems, which required another 19 million rubles. Four thousand people are employed in the development, implementation, and use of various classes of automated management systems (ASU).

In this connection, the legitimate question arises: How effective is this decentralized system of using computer technology and ASU? Unfortunately, as analysis shows, the effect in this case is clearly inadequate. One can enumerate the causes of the reduced effectiveness of ACS.

One of the major causes is inadequate development of the technical equipment complex at computer centers. This increases the costs of information gathering and reduces the reliability of information processing results. Today there is a distinct shortage in the kray of computer centers with operational terminals and hardware for data collection and transmission. Another cause is the shortage of skilled personnel to work at computer centers and in ASU. The personnel problem involves almost the entire network of computer centers. Certain computer centers have 60-70% of the resources needed.

An occasional obstacle is a narrow, departmental attitude toward computer technology funds. As we know, the region has developed a lumber industry complex that combines dozens of large enterprises. The demand for processing their operational and planning information is enormous. A computer information center was established precisely for interaction with all the industry's enterprises in the kray. However, it is guided, and its services are used, only by the VLPO [expansion unknown] of "Krasnoyarsklesprom". The situation, frankly, is paradoxical. The number of workers in this computer information center is almost equal to that in the management apparatus of the association. No efforts are being undertaken to expand the activity of the branch computer information center to the entire lumber industry complex of the region.

What should be proposed? Practice shows that at the present stage of economic development it is impossible to effectively manage the kray's economy without using territorial ASU. An "ASU-Kranoyor'e'" is a vital necessity. Its creation would permit faster and better development of long-term and medium-term integrated programs for the economic development of the kray and its individual industrial regions and branches, as well as design variants for long-term and current plans.

In our opinion, great results could be achieved through the creation of a collective-use computer center (VTsKP), i.e., an independent scientific-production enterprise with a complex of jointly functioning computers, data transmission equipment, and a subscriber network which, together with the appropriate systems and information management software, would allow subscribers, regardless of the office they work in, to make collective use (both locally and long-distance) of the computer resources, programs, and information systems of the CUCC. A collective-use computer center is a highly effective means of saving resources. According to specialists' estimates, VTsKP could reduce service personnel and the costs of hardware.

Solving the problems connected with increasing the impact of the computer technology in use will promote improved management of the economy of the Krasnoyarskiy Kray and, ultimately, an increase in industrial efficiency.

12488
CSO: 1863/5

IMPROVING EFFECTS OF AUTOMATED MANAGEMENT SYSTEMS

Moscow EKONOMICHESKAYA GAZETA in Russian No 40, Oct 83 p 6

[Article by A. Dukhanin, deputy head of the automation department of the "Rezinoproekt" State Design Institute, Moscow]

[Text] The broad automation of production processes has been defined as one of the main directions at work in the resolution of the CPSU Central Committee and the USSR Council of Ministers: "On Measures for Accelerating Scientific and Technical Progress in the National Economy". Taking this into consideration, the creation of automated management systems (ASU) takes on special importance. However, it is no secret that sometimes ASU have little effect. Why?

In our view, the answer lies in imperfections in the organization of work on the creation of ASU. At present, for example, we have not succeeded at all levels in coordinating plans for the development and implementation of ASU with deadlines for construction and start-up of enterprises.

I think that the effectiveness of capital investments in the creation of ASU will improve if the following procedures are established.

Targets for enterprise design are put together by the project client with the assistance of the overall designer on the basis of esimates for this enterprise that are made as part of the development plan for the corresponding industrial branch. Prior to this, there must be a whole complex of work done on the Technical-Economic Basis (TEO) of the automated management systems, and a special ASU developing organization must be designated.

The technical plant (TZ) and TEO are the mandatory source documents for carrying out tasks at the stages of technical and operational design. The schedule of tasks should be coordinated with all interested organizations and balanced with targets for enterprise construction and start-up in accordance with capital construction palns. Together with the approved design plan, the client issues the TZ and TEO for the ASU to the overall design organization, along with other documents.

To promote accelerated implementation of construction tasks, the creators of the ASU use the results of draft work at the TZ stage to issue to the overall

design organization materials for a section on "Automation of production processes and enterprise management".

For these procedures to work out, it should be added in the "General-Branch Methodological Guidelines" (ORMM) that responsibility for introducing the system belongs not only to the client but also the development organization.

A bonus fund for the development organization should be provided only in accordance with developments implemented on the basis of actual economic effectiveness as determined at the test operation stage prior to releasing the system for industrial operation.

12488
CSO: 1863/10

IMPROVING LABOR DISCIPLINE WITH COMPUTERIZED PERSONNEL MANAGEMENT DISCUSSED

Tashkent EKONOMIKA I ZHIZN' in Russian No 7, Jul 83 pp 6-9

[Article by A. Abasov, Deputy General Director for Personnel of the Tashkent Aviation Production Association imeni V.P. Chkalov: "Utilizing Computer Capabilities: The Computer 'Manages' Personnel"]

[Text] The importance of strengthening discipline state, party and production discipline, was again underscored at the June (1983) Plenum of the CPSU Central Committee. This is a problem of first rank importance today. Improving public production efficiency and the quality of all work, and in the final analysis, even the well-being of the Soviet peoples depend to a considerable extent on the successful solution of this problem.

Improving discipline in each area of production activity and at all management levels is just that reserve whose utilization does not require special capital investments, but nonetheless yields a rapid and tangible return.

The work experience of two Tashkent production associations, the aviation production association imeni V.P. Chkalov and "Sredazkabel'" ["Central Asian Cable Production Association"], testifies to this in particular. An automated computerized data retrieval, storage, processing and operational output system for all indicators which characterize the status of labor discipline for each worker, as well as the collectives of shops, departments and the enterprise as a whole has been introduced and is in successful operation at the former. At the latter, an automated continuous quality control system (ASNK) is operating efficiently, which monitors the fulfillment of assignments by the supervisors of each engineering and technical worker. In the last issue of the journal, we briefly informed readers concerning experience of both associations, and today we publish a selection of materials which tell about them in more detail.

The organization of a system for constantly monitoring the status of labor discipline in a collective, as well as the analysis of these data and working out specific measures based on the data to strengthen discipline is one of the most important functions of personnel management. The quality and effectiveness of the planned measures depend to a substantial extent on the presence of the requisite information, its timeliness, completeness and reliability.

Providing such a data using conventional means under the conditions of a large scale enterprise such as the Tashkent Aviation Production Association imeni V.P. Chkalov is practically unthinkable. This task can be handled only by means of modern electronic computer equipment. This is why we have developed and implemented an automated system for the daily retrievel, storage, processing and operational computer output of data on the status of labor discipline of workers, as well as for the collectives of shops, sections and the association as a whole.

Information on violations of discipline and public order are supplied daily from the central attendance time-clock, the safety regulations department, headquarters, voluntary peoples friendship and operational komsomol detachments, are summarized in the personnel department, punched in and transmitted the same day to the computer center.

By morning, data processed overnight at the information computer center for the past day and the cumulative total from the start of the current month is routed to the requisite areas: to all subdivisions of the enterprises, public organizations as well as the general director and his deputies.

The data on violations of public order and labor discipline are printed out by the computer in the form of computer tables. These tables reflect absences, lateness, leaving work early, disruption of conditions within the plant during a shift, petty theft, instances of landing in the "sobering-up" station, minor hooliganism, criminal offences, and a number of others. The workplace and name of the violator as well as the date of the violation are indicated.

Such summaries are used by management at all levels and by party, trade union and komsomol organizations for the analysis and prevention of violations, as well as for taking operationally timely steps to improve labor and production discipline. These data are also the topic of discussion at daily operational production conferences among the supervisors of the subdivisions, the production shiefs as well as at the ten-day and monthly summary conferences of the general director of the association.

The computer tables on the status of labor discipline must absolutely be taken into account in the daily, ten-day and monthly totals for socialist competition as well as when figuring the set contributions of the "thirteenth" wage to the state budget by the enterprise to finance social insurance benefits based on the work totals for the year, and the "fourteenth" for long service.

In line with the procedure which has been developed for determining the totals for the activity of each subdivision, the level of labor discipline is calculated using the formula:

$$Ky = 12V/S$$

where Ky is the level of discipline; V is the number of man-days lost as a result of the violations and S is the average listed number of workers.

This coefficient, expressed as points on a 12 point scale is one of the evaluating indicators in awarding the class standings based on social competition results, and is also reflected in the material incentives for the collectives. For this reason, each of them has a direct interest in routing out cases of violations of labor discipline and law and order from their midst.

The system which has been introduced has become an irreplaceable assistant to the managers of the labor collectives and the specialists in the management of complex production processes. In this case, the advantage of the computer is not just in its capability of storing and reading the data, but also in the fact that it selects and provides information needed by the management and the public organizations for analysis and practical conclusions.

Used along with other measures in the administrative and public areas, the system has a significant impact on curtailing nonproductive losses of worker time, as well as strengthening order and the level of organization in each section.

The social aspect of the functioning system is of no less importance. It consists in the fact that each infraction becomes the topic of discussion and evaluation by all members of the primary labor collective, who are closest to the comrade in their work. All of this promotes the creation of a situation of irreconcilability to violations of norms in our life, an improvement of the level of ideological and moral maturity of the workers, enhances the moral and psychological atmosphere in the collective as well as inculcates in the people a sense of responsibility for the state of affairs in the production work.

The effectiveness of the system can be judged from the following fact: during two months of this year, as compared to the corresponding period in 1982, latenesses and absenteeism were reduced by a factor of 1.6 times in the majority of the subdivisions, while overall work time losses in the association were decreased by more than one-quarter.

It must be said that the strengthening of discipline in the elimination of stoppages during shifts, which dampen the ardor of workers and are one of the reasons for violations, depend in many respects on the labor organization and clear-cut daily shift planning. It makes it possible to precisely account for the labor efficiency of each worker and the collective as a

whole, and to objectively and in an operationally timely manner evaluate their contribution to the common effort.

The organization of daily shift planning is based on the utilization of a computer hardware complex installed at the information computer center and at peripheral shop data processing terminals, which are present in all of the major production shops and affiliates of the association.

The raw data are the plan charts for the shift assignments, covered by the technical control department and turned over by the foreman at the end of the shift to his own punched card terminal. The dual shift operation of these terminals makes it possible to produce decks of punched cards on a daily basis which contain the information on the output and wages. The card stacks are forwarded to the information computer center before 22:00 hours of the current day. They are processed on the computer during the night. By as early as 7:00 AM the next day, the information computer center delivers the computer printouts which account for the volume of daily shift work performed, the calculations of the wages and the bonuses for piece-rate workers to the shops and chiefs of the production operations. Such computer charts are posted for everyone to become acquainted with in each foreman's group. The summary data on a shop by shop basis for the evaluation of work organization quality from the point of view of the foremen are discussed at the daily planning session with the shop chief and serve as the basis for totalling up the competition results.

This system makes it possible to monitor the fulfillment of the assignments by each worker on a daily basis during a shift as well as from the beginning of the month and to allocate the sum of the wages and bonuses to him for those time segments.

The advantage of this organization of the daily shift planning is the fact that it makes it possible, first of all to estimate the labor efficiency of the collectives and each worker in an operationally timely manner, and secondly, to do this completely objectively. The public nature of such an evaluation is also a factor which stimulates the observance of labor and production discipline: if it is your fault and you have lost work time for nothing, the computer figures how many rubles and kopecs this cost you.

Along with the publicity, the system also provides for comparability of the work results of individual workers and collectives as a whole, which is extremely important in improving competition and totaling up its results.

The operational experience of the association in this field has been approved by the Office of the Central Committee of the Uzbekistan Communist Party, and such a high rating is mobilizing our entire collective to search out further reserves for boosting production efficiency. This is all the more necessary because Tashkent aircraft builders are confronted with quite considerable and important tasks. Before the end of the 11th Five-Year Plan, the association collective is obligated to increase production volume by a factor of 1.2 times and labor productivity by a factor of 1.5. In

order to fulfill its promise, we should make more complete use of all available resources, and one of the most important of these was and remains the incessant work on the utmost strengthening of discipline, organization and order.

8225
CSO: 1863/239

IMPROVING AUTOMATED STATISTICAL DATA PROCESSING

Moscow EKONOMICHESKOYE SOTRUDNICHESTVO STRAN-CHLENOV SEV in Russian No 7, Jul 83 pp 67-69

[Article by Valeriy Nazarov, Secretariat, CEMA: "Improving the Automation of Statistical Data Processing". Statistics commentary.]

[Text] The use in the national economy of modern computer technology has opened up new possibilities for radical changes in statistical data processing, deeper economic analysis, and the use of mathematical methods.

This is one of the forms of interaction among the socialist countries within the framework of the CEMA Permanent Commission on Cooperation in the Area of Statistics. By a 1963 decision the Commission set up a permanent working group on the automation of statistical data processing, one task of which was to coordinate the collaboration of the central statistical organs of the CEMA countries in this area and develop appropriate recommendations. At first the group was involved in organizing an exchange of experience in data processing within the statistical organs of the CEMA countries.

Most widespread in these countries at that time were punchcard equipment and first generation computers with a small main memory and low capacity. Such computers could not completely satisfy needs for processing growing volumes of statistical information.

A new stage in the growth of automation in statistical data processing is connected with the appearance of the Unified System (YeS) series of computers, third generation machines.

The statistical organs of the CEMA countries are quickly being equipped with these installations. At present these computers make up the entire inventory of computers in a number of countries, and over 75% in others. The availability of similar computers operating on common principles provided real prerequisites for a transition from solving individual statistical problems to integrated systems of statistical data processing--the organization of automated systems of state statistics (ASGS).

Along with the growth of the computer network of the statistical organs of the CEMA countries came improvements in the activity of the permanent working group on the automation of statistical data processing.

The basis of the group's activity at present is multi-faceted collaboration for the improvement of planning and building integrated ASSS and their individual elements.

The ASGS is a system of collecting and processing statistical information for the planning and management of the economy that ensures the broad use of mathematical, economic and statistical methods with the utilization of electronic and other computer technology, and communications media in the organs of state statistics. The goal of ASGS is first of all to significantly broaden the reference capability of state statistical agencies without increasing reporting and to upgrade the timeliness and reliability of the output data necessary for managing the national economy. The system also provides for shortening the time needed to prepare bookkeeping documents while reducing expenditures of labor and materials.

The establishment of ASGS in the CEMA countries is considered a major trend in the development of statistical information systems. For this purpose, new forms of organizing statistical information processing are being introduced, and existing ones improved, in functioning computer centers (CC). Present software is being modernized and new software created; overall system design materials are being issued to regulate a unified approach. Statistical data processing with the aid of telecommunications (teleprocessing) is finding wider and wider implementation in the practical work of central statistical agencies. An automated data bank (ADB) is being utilized.

Powerful CC are in operation, equipped with modern computers, technology for long-distance data transmission, and duplication and other necessary equipment. There are computer centers at central and peripheral statistical agencies. For example, the system at the USSR Central Statistics Administration has a four-level hierarchical organization of computer centers: a Union, republic, oblast, and rayon level. In Bulgaria CC operate on two levels; central and outlying CC have been charged with the duties of collecting, processing, and transmitting statistical information in two directions: horizontally, for the support of local management agencies, and vertically, for transmission to CC of higher statistical agencies.

In this way the entire flow of statistical information is concentrated at computer centers and distributed by them, while the central agencies of government statistics provide methodological guidance for statistics within countries.

Moreover, CC perform composite information processing for ministries and departments, enterprises, kolkhozes, sovkhozes, and other organizations, fulfilling the function of a collective-use computer center.

In all the CEMA countries there is a rapid growth in the production capabilities of CC, an increase in the number of problems being solved, and increased demands on the quality of statistical information and the speed with which it is made available. All this calls for an integrated approach to the management of computer processes and the international division of labor in the creation of data processing systems.

There has been an expansion of multi-faceted collaboration among the CEMA countries in the area of automated processing of statistical information.

This collaboration is directed towards finding a unified approach to the design of ASGS, further improvements in the hardware, software, and information and organizational support of ASGS, and the standardization of technical documentation.

In collaboration on automated processing, problems that can be solved in the same way for all CEMA countries are becoming more and more important.

Bearing in mind that in the individual CEMA countries a significant portion of the computer inventory is made up of Unified System computers, the permanent working group is studying and applying work experience with these computers, recommending more effective uses, and rational division of labor among the CEMA countries in the design of laborious areas of work on the creation of ASGS.

A number of key methodological materials on automating statistical data processing have been developed and coordinated. One of the important links in ASGS is the creation and implementation of ADB, which is its subsystem. In consideration of the importance and complexity of the problem of creating ABD in the CEMA countries, the CEMA Permanent Commission on Collaboration in the Area of Statistics has ordered the working group to develop three interrelated documents: principles of creating and using ADB, technical specifications for the creation and use of ADB, and standard specifications for the creation and use of ASGS ADB with the use of Unified System computers. The work was coordinated by the delegation from the GDR, with the active participation of delegations from Bulgaria, Hungary, the Republic of Cuba, Mongolia, Poland, the USSR, CSSR, and Yugoslavia. The foundation was an analysis of the experience of the CEMA countries in view of prospects for the development of automated systems of state statistics in the survey period. The aim of the project is to promote the creation of new ADB and improve existing ones according to a unified methodology, which will ensure the future interaction of CEMA countries' ASGS. The document successfully develops materials suitable for widespread use not only in statistics but also in the practical work of various branches and departments.

A joint effort is being made at present to develop the theme "Creation and Use of Distributed ADB for ASGS with Unified System Computers". This bank is a system of interacting local ADB having common methodological and information principles, software, and hardware and joined by a system of long-distance data transmission (teleprocessing). Introduction of these systems will permit inclusion of all existing CC in the system of state statistical agencies in a single network.

A number of methodological documents on the automation of processing statistical materials have been developed. One of them--"A Model Flow Chart for Data Collection and Processing in ASGS"--is extremely important for the design of processes in ASGS based on Unified System computers. The chart utilized the countries' experience, which in many ways predetermined its methodological and technical solutions. It includes the basic devices and

methods used to realize problems in the collection, recording, checking, transmission, storage, processing, input and output of information, as well as procedures for using equipment for its effective utilization.

A dictionary has been compiled containing the basic terms and concepts for creating a unified language of communication for all CEMA countries on automated statistical systems. The main executor of both documents was the USSR delegation.

The active participation of the USSR and CSSR delegations was involved in the development of Procedural Statements on the creation of ASGS system program software; these include overall conception, basic directions and content for developing system program software, recommendations on the make-up of applied program packets for statistics and the principle of using them, and introduction of a catalog of ASGS applied programs and procedures for modifying applied programs.

Also created and coordinated was a Flow Chart for a System of Automated Documentation (data output) for Unified System computers on ASGS program software. The system is a package of applied programs whose use will free designers from the need to program procedures for formatting output data in the form of corresponding charts. The package has been developed as a hierarchical tree module system composed of a specialized monitor of master programs and a set of modules. Such a structure ensures the independence of modules and permits step-by-step development of the package and the possibility of step-by-step utilization.

With the active collaboration of the other delegations, the delegations from Hungary and the USSR, acting as main executors, developed a Procedural Guide for choosing hardware for the collection, transmission, processing, and output of information for collective-use computer centers and remote user sites. The document treats the organization of information processing at these centers, the time it takes to respond to user queries, and the organization of a multiprogramming information processing mode, and makes recommendations on the choice of computers, devices for data preparation, and copying equipment.

Furthermore, the permanent working group on the automation of statistical data processing devotes considerable attention to ASGS organizational software. Thus, the delegations from Hungary and the CSSR, with the participation of the other delegations, have developed Basic Principles of ASGS Organizational Software.

The authors of the Basic Statements on the Structure and Content of ASGS Technical Documentation were the delegations of the USSR and the CSSR. The technical documentation here serves to unify all the elements that make up the ASGS.

The Hungarian delegation in the Commission as chief designer presented a System for Storing and Recording Data and Documentation in ASGS. This system reflected the optimal variant for the construction and content of a system

for storing and recording data and documentation. Thus, the statistical agencies of the CEMA countries are achieving unification of their information retrieval services and systems for recording data and documentation.

In addition, within the framework of the Commission, the following topical methodological materials on problems of the automation of statistical data processing have been developed and coordinated:

theoretical principles of the integration of information systems;

a system for teleprocessing operational statistical information for the fulfillment of a plan at the regional and central levels;

a decentralized system for processing statistical information on the basis of minicomputers;

basic principles of safeguarding information in the ASGS computer center network;

a plan for organizing a distributed ASGS automated data bank;

basic statements on the management of the computer network of the statistical agencies of the CEMA countries; etc.

Another characteristic example of the multi-faceted collaboration of the CEMA countries is the integrated development of a Commission for Procedural Materials on automated data processing for general and sample censuses and population surveys.

Recommendations have been developed and approved for the use of non-punch storage devices for input of raw data, automatic checking and correction of census data, unified standard programs for processing census materials, methods of organizing data files, development of ready-made charts, and more.

At present computer technology is constantly improving: main and external memories are being expanded and the speed of information processing accelerated. In this regard, there have also been improvements in the methods of processing information using this technology and in its mathematical software, and the sphere of computer applications is growing.

This will enable us to arrange the exchange of information between computers, the so-called data transmission or teleprocessing system. The combined use of computers and data transmission systems opens up long-range avenues for collective use of computer technology and, on this basis, the creation of large territorial computation systems. The latter ensure easy long-distance access to computer resources and joint exploitation by many users, eliminating the need for each to have his own computer technology.

The multi-faceted collaboration of the CEMA countries for the improved automation of statistical data processing is yielding tangible benefits. There

is mutual enrichment of the theory and practice of planning and implementing automated systems of state statistics and a reduction of expenditures on their development. Economic and mathematical methods are being more widely applied, statistics methodology is being improved, and the quality of statistical information is rising.

12488
CSO: 1863/9

AUTOMATED PROCESSING IMPROVES ACCOUNTING AND ANALYSIS

Moscow EKONOMICHESKAYA GAZETA in Russian No 39, Sep 83 p 16

[Article by N. Grudinin, deputy director for economic affairs, sovkhoz imeni Lenin, and A. Vasil'yev, chief bookkeeper: "Efficiency of Accounting and Analysis: Automated Processing of Accounting Information"]

[Text] It has already been two years since the sovkhoz imeni Lenin, Lenin Rayon, Moscow Oblast, has converted completely to automated processing of accounging information. Computation of wages, benefits, additional payments, and a number of other jobs is carried out in automated fashion.

The system of machine information processing was implemented by specialists from the Lithuanian branch of the All-Union State Polytechnical Institute of the USSR Central Bureau of Statistics, whose consultative help we continue to use today.

What does automated processing offer us? First of all, it replaces and makes easier the routine work of bookkeepers through the use of machines; the ability to analyze accounting data can be expanded to the desired limits with no difficulty. The ease of analyzing information allows us to make various kinds of management decisions in a timely way, which has a positive impact on production.

The accounting apparatus has been restructured on the initiative of the bookkeepers themselves. Separate groups of bookkeepers have been set up in accordance with the conditions of automated processing of accounting information. Thus, there is a separate group for the accounting, and labor accounting. The labor accounting group employs only five bookkeepers instead of eleven. But today we are concerned about questions of the expanded application of computers. Why not use computers to obtain, say, ready planning estimates, like the balance that we now obtain? How can we transfer to this machine the jobs of drawing up accounts and carrying out compoiste analyses? After all, the same norms for output and valuation and norms for expenditures on fuel and lubricants, used in accounting and input into the computer's memory, are used in drawing up flow sheets.

This is why the automation of flow sheet compilation and monitoring of adherence to those flow sheets is a priority task; for this will enable us to

conduct integrated processing of economic information on the basis of unified normative reference information and to use the derived data to discover new production reserves within the production technology. In practice there are frequent cases when individual subdivisions within the national economy allow significant losses to occur in the harvest due to breakdowns in production technology. And sometimes, because of a lack of appropriate controls, these losses go unnoticed and no one bears responsibility for them. It is extremely difficult to implement such controls using manual information processing. Therefore, we believe that computers should come to our aid in such cases.

A laborious part of economic work is economic analysis. Especially large labor expenditures are required for collecting and grouping data and computing various indices. In our view, this area of economic work should also use computers.

In our farm a rather labor-intensive area of accounting work is the preparation of financial documents for their inclusion in a bank encashment for goods sold and services rendered. During the strawberry-harvesting period, our farm sends its produce out to some 200 enterprises every day; it is therefore very difficult to draw up this quantity of accounting documents manually. Documents for encashment are written up every day; therefore, all calculations for the preparation of documents for encashment must be carried out manually, while computers are used in these operations only for the automated reflection of data in accounts of synthetic and analytical accounting. We believe that the primary data on the realization of production should be fed into the computer every day, and after the appropriate data processing, the computer should print the necessary financial documents for encashment at the bank.

An especially urgent question at present is the struggle with losses of working time. Information on losses is needed not only for the categories and professions of workers but also for each worker, for particular reasons. However, such data are not being accumulated in the bookkeeping system. The use of computers in processing data on losses of work time could have a positive effect on work discipline.

However, the capabilities of computers in this area of bookkeeping are also unexploited to date. Practice shows that only the widespread use of computers and the organization of composite, integrated automated processing of economic information from all sectors of agricultural production will enable us to achieve the highest economic impact from the use of computers.

For example, if our farm processes automatically only bookkeeping information, while the conduct of economic analyses, the compilation of planning estimates, and the processing of other kinds of economic information are carried out manually, as before, then we cannot expect a more significant effect from the use of computers to process bookkeeping information alone. The efficacions solution of management problems requires not only bookkeeping information, but at the same time other kinds of economic information as well.

We fully approve the initiative of the All-Union State Polytechnical Institute of the USSR Central Bureau of Statistics to establish an experimental computer center at our farm. But we would like the work that has begun here in the automation of economic information processing to continue to develop.

12488
CSO: 1863/10

COLLECTIVE-USE COMPUTER CENTERS CREATED IN UKRAINE

Moscow VESTNIK STATISTIKI in Russian No 8, Aug 83 pp 22-24

[Article by I. Iskra, deputy director, Ukrainian SSR TsSU [Central Statistical Administration]]

[Text] The statistical administrations and computer centers of Lvov and Vinnitsa oblasts and the Republic Computer Center of the Ukrainian SSR TsSU, guided by measures resulting for government statistical agencies from the decisions of the 26th CPSU Congress and subsequent plenums of the CPSU Central Committee and the Central Committee of the Communist Party of the Ukraine, are doing work on creating collective-use computer centers in the cities of Kiev, Lvov and Vinnitsa.

For the purpose of solving a number of organizational problems relating to the creation of VTsKP's [collective-use computer centers], the Ukrainian SSR Council of Ministers has entrusted the Lvov and Vinnitsa oblispolkoms and the Kiev gorispolkom of Councils of People's Deputies to take this work under their supervision and to render active assistance to statistical agencies. In executing this order, the Lvov and Vinnitsa oblispolkoms have approved a list of user organizations, measures for selecting personnel, the makeup of the repair and construction organizations for re-equipping and adapting production areas, etc. In addition, under the auspices of the Vinnitsa oblispolkom a coordination council has been created for solving scientific methodological and practical problems relating to the creation of VTsKP's, and under the auspices of the Lvov gorkom of the Communist Party of the Ukrainian SSR, a technical and economic council.

Questions relating to the creation of VTsKP's are under the constant supervision of the Ukrainian SSR TsSU and progress in the fulfillment of working and calendar plans is regularly reviewed and discussed in a scientific and technical council, in boards of the Ukrainian SSR TsSU and statistical administrations, and at conferences held by the Ukrainian SSR TsSU together with specialists of computer centers and the appropriate planning organizations.

It is necessary to note that measures whose performance was called for for 1981-82 have basically been fulfilled. No small difficulties have been caused by the problem of selecting and outfitting the staff of computer centers with specialists in connection with the appearance of new computer

facilities. Additional measures have been taken to improve the quality structure of specialists of existing computer center departments, with respect to programming of engineering and technical problems, as well as to outfitting the staffs of specially created subdivisions of VTsKP's and reinforcing with specialists subdivisions of the Ukrainian branch of the USSR TsSU VGPTI [All-Union State Design-Technology Institute].

At the present time 90 people are already working at computer centers on the problem of creating VTsKP's, including 52 people at the Republic Computer Center of the Ukrainian SSR TsSU, 16 people at the computer center of the Lvov Oblast Statistical Administration, and 22 people at the computer center of the Vinnitsa. In 1982, 38 specialists were trained through the teaching centers of the "Algoritm" [Algorithm] special scientific production association and other organizations, and the plan is to train 72 more people in the current year.

In keeping with the "Coordination Plan for Development of a System Complex for On-Line Monitoring and Analysis of the Fulfillment of National Economic Plans," work is being done relating to interaction of the Ukrainian SSR TsSU ASGS [Automated System for State Statistics] and the Ukrainian SSR Gosplan ASPR [Automated Control System for Planning Calculations]. The Ukrainian SSR TsSU RVTs [Republic Computer Center] in conjunction with the Ukrainian SSR Gosplan State Computer Center and the Ukrainian branch of the USSR TsSU VGPTI have developed a data base for statistical reporting indexes, for form No 1-p (kind) and form No 1-p (cost) under the control of the "OKA" SUBD [data base management system]. Kind indexes are being transmitted to the Ukrainian SSR TsSU RVTs from the computer centers of oblast administrations through switched telephone communication lines. The data bases enable access of Ukrainian SSR Gosplan personnel to them.

It is planned in the future to develop and manage data bases for statistical reporting indexes completely characterizing scientific and technical progress and the economic activity of industrial enterprises, including machine building, light industry, agricultural production and volume of purchases, as well as for labor statistics.

The Ukrainian SSR TsSU, in creating VTsKP's in the cities of Kiev, Lvov and Vinnitsa, has it in mind to make maximum use of them for statistical needs and primarily for purposes of further reducing the time required for developing statistical reports, including routine and situation reports, to improve their quality and to raise economic work to a higher level.

Work is being actively done with the users of the VTsKP's being planned. Statistical administrations and their computer centers and the Ukrainian SSR TsSU RVTs have precisely determined the makeup of user organizations. One hundred and six organizations, including 52 in Kiev, 21 in Lvov and 33 in Vinnitsa, will comprise the total makeup of users of the first phase of VTsKP's. Contracts for the development and introduction of tasks have been concluded with the majority of them (80 percent). Integrated tasks are being planned by computer centers and the Ukrainian branch of the USSR TsSU VGPTI in keeping with approved plan schedules.

In the past 2.5 years statistical administrations and computer centers have provided for the completion of work on preparation of production areas for installing computers and other production equipment. Repair work for preparing the production area has been completed and a YeS-1035 computer has been installed at the computer center of the Lvov Oblast Statistical Administration. Work on preparing areas at the Ukrainian SSR TsSU RVTs and at the computer center of the Vinnitsa Oblast Statistical Administration is in the stage of completion. Design documentation has been developed for a number of sections of the detail and contract design, and engineering assignments for the creation of VTsKP's, design documentation for the construction of communication channels, designs for the hardware of VTsKP's and user stations, as well as norm-setting documentation relating to questions of the operations of VTsKP's of the Ukrainian SSR TsSU system have been approved. The USSR TsSU VGPTI has already completed development of the design for the hardware and software of VTsKP's.

In the time which has passed, computer centers have acquired and at the present time have available a practically complete fund of recommended software. The operating system has been introduced at all three VTsKP's and the "Kama" teleprocessing system is being mastered. They have already begun to try out the teleprocessing mode at the Ukrainian SSR TsSU RVTs.

Soon this mode will be tried out at the computer centers of the statistical administrations of the cities of Lvov and Vinnitsa (after entry into service of YeS-1035 computers).

In the meantime, there are also difficulties in the job of creating VTsKP's, relating particularly to the implementation of plans for the organization of communication channels for VTsKP users in Kiev. Changes in the plan for furnishing VTsKP's with 2-computer complexes have caused considerable complexities. It was necessary on short notice to change the design documentation and the direction of work on the reconstruction of areas. Now it is urgently necessary to solve the problem of furnishing the Ukrainian SSR TsSU RVTs and the computer centers of the Lvov and Vinnitsa oblast administrations with motor generators, since in the process of debugging the YeS-1045 and YeS-1035 computers it was found that the stability of the supply voltage of substations does not satisfy the specifications of the computers. Unfortunately, there have been cases of deliveries of equipment (AP-63's and MPD-2's) later than the planned deadlines, not called for by the project, etc., which could not not have an effect on timely entry of equipment into service.

Remaining to be desired is better organization of work relating to the discussion and coordination of design documentation developed by the USSR TsSU VGPTI. It is already now necessary to enlist the Ukrainian branch of the USSR TsSU VGPTI more actively in the problem of creating VTsKP's, which will make it possible for it to take an active part in work relating to introduction and will shorten the times required for development as a whole.

8831
CSO: 1863/4

IMPROVING ACCOUNTING FOR MAGNETIC INFORMATION MEDIA AT COMPUTER CENTERS

Kiev EKONOMIKA SOVETSKOY UKRAINY in Russian No 7, Jul 83 pp 88-90

[Article by V. Nazarchuk]

[Text] One important direction of scientific and technical progress enabling conformity of forms of organization and management methods to the modern level of development of production forces is automation of control of the national economy at all of its levels. An important role in this task belongs to computer centers (VTs's) furnished with modern high-speed computers.

Third-generation computers have become widespread at the present time, which has resulted in a growth in the amount of computer information media used and consumed. Typical of this process is the fact that the number of magnetic information media (magnetic tape, magnetic disks, etc.) used at computer centers is growing at a rapid pace as compared with punched media (punched cards and punched tape). On the republic scale the cost of magnetic media used equals millions of rubles and in connection with the termination of the production of punch card equipment in this five-year plan period it will increase considerably more.

Of course, under these conditions the problem of the efficient and economic utilization of these material resources and, primarily, accounting for them, is a pressing one.

However, as demonstrated by a sampling study conducted by us of a number of computer centers of the republic's ministries and departments, the solution of these problems in accounting practice cannot be considered satisfactory. It must be said that this problem, although requiring a special theoretical study, at the present time has not been duly reflected in the literature and in practice even unified instructions for all computer centers on accounting for magnetic media are lacking.

Therefore, some ministries and organizations having a great number of computer centers have developed their own departmental instructions for accounting for magnetic media (USSR Minpribor [Ministry of Instrument Making, Automation Equipment and Control Systems], USSR TsSU [Central Statistical Administration], etc.). Similar developments and instructions have been

lacking up to the present time at computer centers of other systems, as the result of which accounting for magnetic media (especially disk packs) at computer centers is carried out by quite varied methods.

For example, magnetic tape in the accounting practice of computer centers comes under the heading, as a rule, of the group of low-value items which wear out quickly. The basis for categorizing magnetic tape under this group is its limited service life--about a year--as well as its low cost (the cost of a reel is less than 100 rubles). Moreover, in practice two different variants are used for attributing the cost of magnetic tape to products produced by the computer center and services performed. The majority of computer centers, in transferring magnetic tape to use, credit 50 percent of the wear and the remaining 50 percent is finally credited when the tape is written off as the result of wear (60,000 to 70,000 meters run). At other computer centers (e.g., in the USSR Minpribor system), according to the instructions for accounting for magnetic tape*, when it is released from the storeroom for use the wear is credited to the tune of 100 percent and is attributed to performance of computing and scientific research work. After the work is performed for which the tape was issued, in case of its suitability for further use it should be temporarily stored in the storeroom, and the remaining cost of the tape is written off from expenses for the specific job to which it had previously been attributed to the tune of 100 percent.

The above-described two methods of accounting for magnetic tape have their inherent disadvantages. In the first case when 50 percent of the original cost is written off, it is difficult to distribute this cost among the tasks (orders) in the performance of which the tape was used. In the second case, when 100 percent of the tape's wear is credited at the moment it is transferred to use and a determination is later made of actual wear, with this process reflected by appropriate adjustment entries, the disadvantage inherent in the first method is eliminated. On the other hand, organization of accounting for magnetic tape according to the second method is considerably more complicated.

An improved method of accounting for the wear of magnetic tape which can be suggested for application in practice is based on the use of norms for its wear. In developing such norms it is necessary to start with the service life of the tape (similarly to fixed capital), taking into account the intensity of its use. The following can be indicators of the intensity of use of tape: the number of references to the tape in the process of solving problems (processing data); the number of installations (removals) of tape per unit (tape storage); and the number of tape runs. Having a norm for tape wear determined on the basis of the above-listed indicators, it is possible with a sufficient degree of accuracy to determine the total wear and write off these expenses for the jobs in which the tape was used.

*BUKHGALTERSKIY UCHET [ACCOUNTING], No 11, 1975, p 72.

In addition to magnetic tape, at the present time magnetic disks--packs of replaceable magnetic disks--are widely used, the use of which enables more rapid interchange of information with the computer, which has mainly been responsible for their wide use at computer centers.

In terms of their cost, as well as the nature of their use, magnetic disks represent one of the important resources of a computer center. However, accounting for them under conditions of the lack of unified instructions on this question is not the same at the computer centers of different ministries and departments.

In realizable assets accounting magnetic disks are categorized under various groups. At some computer centers disks are taken into account as fixed capital. The justification for attributing magnetic disks to fixed capital in accounting is in this case their high cost--more than 300 rubles--and a service life greater than one year.* In this case depreciation is credited for them as for other fixed capital. However, the depreciation standard used for magnetic disks at various computer centers is not the same. Other computer centers account for magnetic disks similarly to magnetic tape, attributing them in accounting to low-value items which wear out fast. Also encountered is the variant of accounting for disk packs as spare parts.

The absence of validated theoretical research on the question of accounting for these realizable assets of a computer center does not make it possible totally to justify or reject a specific accounting variant used in practice. However, in our opinion in solving this problem it is necessary to pay attention to not only the role of magnetic disks in the production process (in terms of their role, magnetic disks are labor resources and therefore should be accounted for among fixed capital), but also the nature of their use. In this case the use of magnetic disks at computer centers is somewhat similar to the use in industry of special expensive tools. Therefore, in accounting, magnetic disks can come under the heading, in our opinion, of low-value items which rapidly wear out.

This position can be corroborated by the following. A computer has a limited (fixed) number of drives into which disk packs are placed. In the process of solving a problem, the situation can arise when more or less than the available number of units are required. If less of them are needed, then one of the units is not used in solving this problem. And if more of them are needed (depending on the amount of information to be processed), then one of the units (or more) is stopped in the process of operation and the disk pack in it is changed. We can observe an analogous situation at an industrial enterprise in the process of machining of parts, e.g., on a multispindle lathe where various numbers of cutting tools are required. Cutting tools are changed depending on the kind of machining (roughing, finishing, and the like).

*"Preyskurant No 17-08. Optovyye tseny na sredstva vychislitel'noy tekhniki" [Price List No 17-08. Wholesale Prices for Computer Technology Facilities], put into effect as of 1 January 1982.

The difference in these processes between a cutting tool and a replaceable disk pack will consist only in the fact that the cost of the latter can be considerably higher than the cost of the cutting tool.

In determining norms for the wear of magnetic disks, it is necessary to start with the service life, which depends on the number of references to the replaceable disk pack and the number of installations/removals. Practically speaking, there are no other indicators when working with a pack, since, unlike tape, if a pack is installed then in the working position it is in constant motion and does not stop during an idling period. Thus, for the purpose of arriving at standard indicators for the service life of these low-value items which wear out rapidly (magnetic tape and disks), it is necessary in accounting practice to have data on the nature of their use. It turns out that there is no need to install special measuring devices and counters for these purposes. Practically all computers are capable of automatically counting the number of references to magnetic storage units, the number of installations and removals, and the like. It is necessary only to utilize this capability in practice.

Proper calculation and attribution of the total wear of magnetic tape and disks to each problem solved on the basis of norms for wear will make it possible to determine more precisely the cost of each task and will be conducive to the further reinforcement of cost accounting at computer centers, making possible the economic utilization of expensive realizable assets.

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COMPUTER ON THE PHONE

Kishinev SOVETSKAYA MOLDAVIYA in Russian 21 Aug 83 p 4

[Article by B. Gisser, ATEM correspondent]

[Text] A computer has been plugged into service staff "09" of Kishinev's municipal telephone station. It can find the right number, as they say, in the wink of an eye.

All one has to do is key in one's last name, and a home telephone number appears immediately on the screen. Finding the number among the numbers of almost 100,000 "call-number" subscribers in the city that have been recorded on magnetic disks takes just 0.18 seconds.

With almost the same speed the computer can give the telephone numbers of plant services, even when names of enterprises have been shortened or replaced by abbreviations for the sake of rapid inquiries. It can also be used to "leaf through" on the screen lists of phone numbers of stores, drugstores, movie theaters, hotels...

These are the capabilities of the country's first ASS-09, an automated system for information service. Its computer can serve over 30 workplaces at the same time. For now, a smaller number of displays is sufficient for the city. The first ones are already in operation, and the people of Kishinev do not even suspect that many of their questions addressed to telephone operators using the new equipment are quickly answered with the aid of a computer.

Full implementation of the automated system will render unnecessary the traditional manual card files used by information subdivisions. There are now two such files at every workplace: one holds cardboard cards with office phone numbers, the other--home phone numbers. So operators must go through these cards to find the number of the user. And during a shift each operator receives no fewer than 800-900 inquiries.

T. Serbinova, manager of the 09 service, says:

"The card files are filed and corrected by hand. If we consider that the city is introducing new telephone exchanges and expanding existing ones, and

there are changes in the addresses of organizations and residents and the names of streets, it is not hard to imagine how complicated it is to deal with these everyday changes on an operational basis. And we have to listen to complaints about slow service on the part of our workers. And on days when someone is sick, work is even harder. The automated system will make operators' work considerably easier and increase the reliability of information. This will also be an advantage to those who request that we find the number of a subscriber. And it will be easier to dial the number of our service."

The authors of the system, specialists in the department of mini- and microcomputer systems at the Kishinev construction design bureau for automated control systems, have noted an interesting fact: it took only four minutes to replace an old street name with a new one in the computer data bank that is now the common card file for all telephone operators.

I. Buzhilov, head of the Kishinev municipal telephone station, says the following about the merits of the system that was awarded a certificate at the "Automation-83" international exhibition:

"We have the possibility of issuing in the near future a new telephone directory, literally with cosmic speed. The computer needs only four hours to transfer the entire data bank onto magnetic tape. In the same amount of time, a printing house photosetter could use this tape to prepare an edition for print. It used to take over a year just to compile a directory."

"Creating an automated system," continued the head of the municipal telephone station, "will allow our information service in the near future to introduce so-called service maintenance for subscribers. They will be able to receive telephone information about the schedules of trains, planes, and inter-city buses, features at theaters and movies houses, and addresses of specialized stores. The program for such service has already been prepared."

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